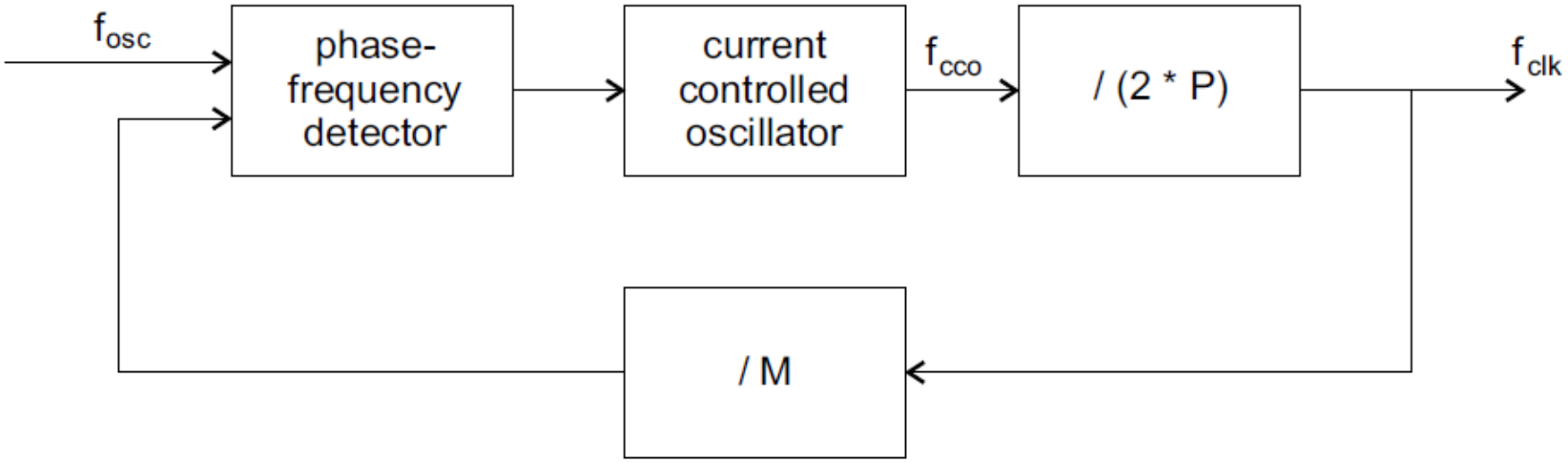
Vaja2
Inicializacija hitrosti ure procesorja (fclk) in perifernega vodila (fvpb)

1. Izpišite trenutne vrednosti za fclk (fvpb)
2. V neskončni zanki preverjajte stanje tipk:
    - T0 naj poveča fclk (do max. 60MHz
    - T1 naj zmanjša fclk (do min. 12MHz)
3. Dodatek
    - T2 naj poveča fvpb (do max. fclk)
    - T3 naj zmanjša fvpb (do min. fclk/4)



Slika B.3: Fazno sklenjena zanka

$$\begin{array}{rcccl} 10\text{MHz} & \leq & f_{osc} & \leq & 25\text{MHz} \\ 156\text{MHz} & \leq & f_{cco} & \leq & 320\text{MHz} \\ 10\text{MHz} & \leq & f_{clk} & \leq & 60\text{MHz} \end{array} \qquad \text{(B.1)}$$

fosc=12MHz

$$\begin{aligned} f_{cco} &= 2 \times P \times f_{clk} \\ f_{clk} &= M \times f_{osc} \end{aligned} \qquad \text{(B.2)}$$

Table 13: PLL registers

Name	Description	Access	Reset value[1]	Address
PLLCON	PLL Control Register. Holding register for updating PLL control bits. Values written to this register do not take effect until a valid PLL feed sequence has taken place.	R/W	0	0xE01F C080
PLLCFG	PLL Configuration Register. Holding register for updating PLL configuration values. Values written to this register do not take effect until a valid PLL feed sequence has taken place.	R/W	0	0xE01F C084
PLLSTAT	PLL Status Register. Read-back register for PLL control and configuration information. If PLLCON or PLLCFG have been written to, but a PLL feed sequence has not yet occurred, they will not reflect the current PLL state. Reading this register provides the actual values controlling the PLL, as well as the status of the PLL.	RO	0	0xE01F C088
PLLFEED	PLL Feed Register. This register enables loading of the PLL control and configuration information from the PLLCON and PLLCFG registers into the shadow registers that actually affect PLL operation.	WO	NA	0xE01F C08C

[1] Reset value relects the data stored in used bits only. It does not include reserved bits content.

Table 16: PLL Status register (PLLSTAT - address 0xE01F C088) bit description

Bit	Symbol	Description	Reset value
4:0	MSEL	Read-back for the PLL Multiplier value. This is the value currently used by the PLL.	0
6:5	PSEL	Read-back for the PLL Divider value. This is the value currently used by the PLL.	0
7	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA
8	PLLE	Read-back for the PLL Enable bit. When one, the PLL is currently activated. When zero, the PLL is turned off. This bit is automatically cleared when Power-down mode is activated.	0
9	PLLC	Read-back for the PLL Connect bit. When PLLC and PLLE are both one, the PLL is connected as the clock source for the microcontroller. When either PLLC or PLLE is zero, the PLL is bypassed and the oscillator clock is used directly by the microcontroller. This bit is automatically cleared when Power-down mode is activated.	0
10	PLOCK	Reflects the PLL Lock status. When zero, the PLL is not locked. When one, the PLL is locked onto the requested frequency.	0
15:11	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

Table 27: VPB Divider register (VPBDIV - address 0xE01F C100) bit description

Bit	Symbol	Value	Description	Reset value
1:0	VPBDIV	00	VPB bus clock is one fourth of the processor clock.	00
		01	VPB bus clock is the same as the processor clock.	
		10	VPB bus clock is one half of the processor clock.	
		11	Reserved. If this value is written to the VPBDIV register, it has no effect (the previous setting is retained).	
7:2	-	-	Reserved, user software should not write ones to reserved bits. The value read from a reserved bit is not defined.	NA

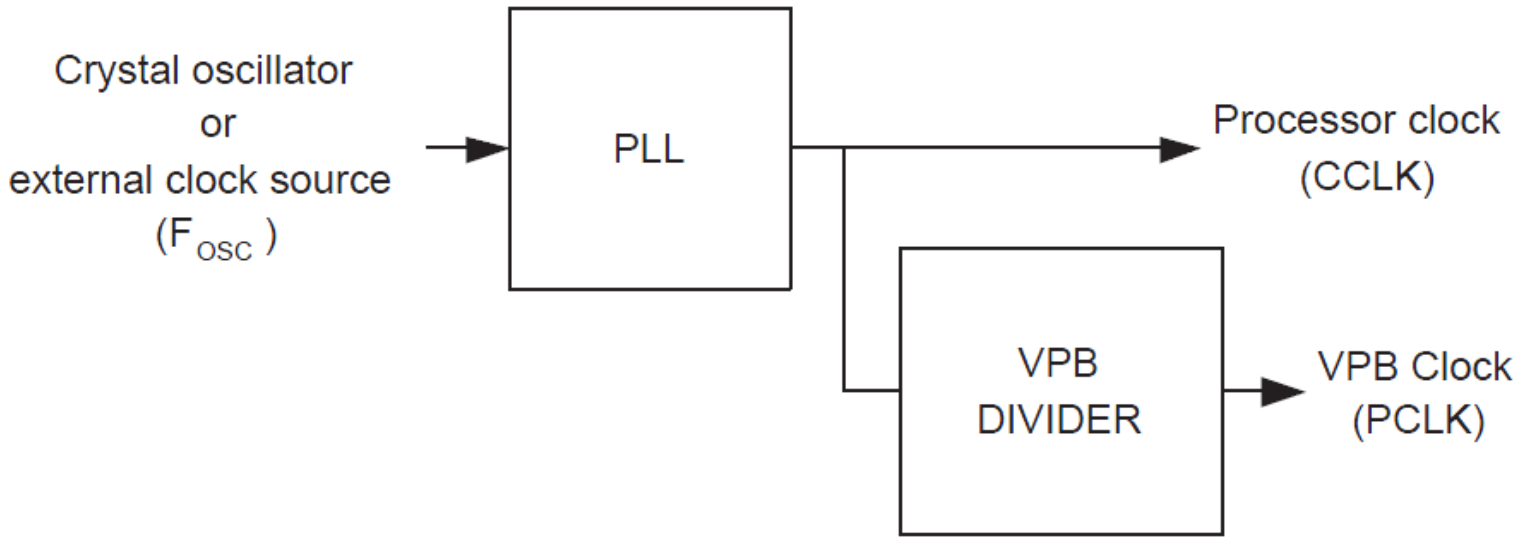


Fig 12. VPB divider connections

$$\begin{array}{rcccl} 10\text{MHz} & \leq & f_{osc} & \leq & 25\text{MHz} \\ 156\text{MHz} & \leq & f_{cco} & \leq & 320\text{MHz} \\ 10\text{MHz} & \leq & f_{clk} & \leq & 60\text{MHz} \end{array} \quad \text{(B.1)}$$

fosc=12MHz

$$\begin{aligned} f_{cco} &= 2 \times P \times f_{clk} \\ f_{clk} &= M \times f_{osc} \end{aligned} \quad \text{(B.2)}$$

PLLSTAT : xxxx .... xxxx x p1 p0 m4 m3 m2 m1 m0

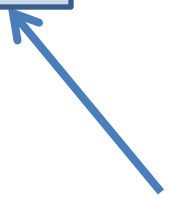
M-1

bit6	bit5	P
0	0	1
0	1	2
1	0	4
1	1	8

Tabela B.1: Vrednosti konstante P

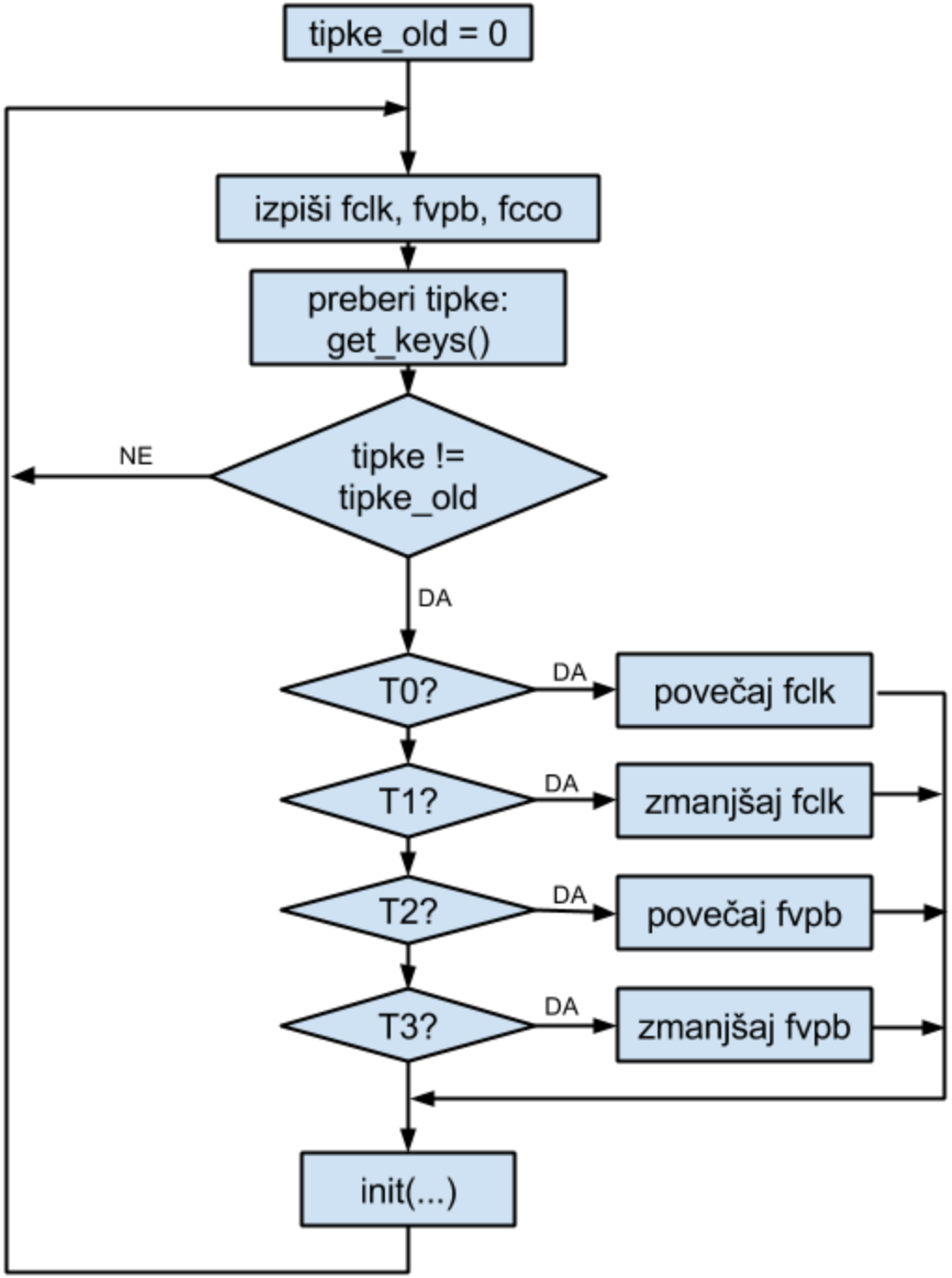
VPBDIV : xxxx …. xxxx xx n1 n0

fvpb=fclk / n



bit1	bit0	
0	0	$f_{clk} = 4 \times f_{vpb}$
0	1	$f_{clk} = f_{vpb}$
1	0	$f_{clk} = 2 \times f_{vpb}$

Tabela B.2: Delilno razmerje med urinima signaloma f_{clk} in f_{vpb}


tipke_old = 0
izpiši fclk, fvpb, fcco
preberi tipke:
get_keys()
tipke !=
tipke_old
NE
DA
T0?
DA
povečaj fclk
T1?
DA
zmanjšaj fclk
T2?
DA
povečaj fvpb
T3?
DA
zmanjšaj fvpb
init(...)