Laboratorij za načrtovanje integriranih vezij

UNIVERZA V LJUBLJANI
Fakulteta za elektrotehniko

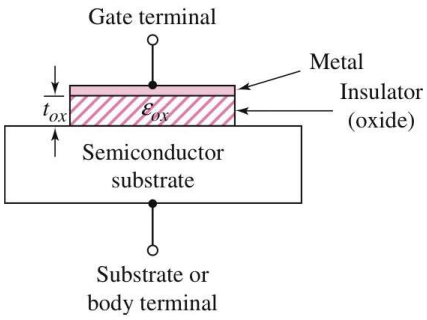
Linearna elektronska vezja

Osnove tranzistorjev FET

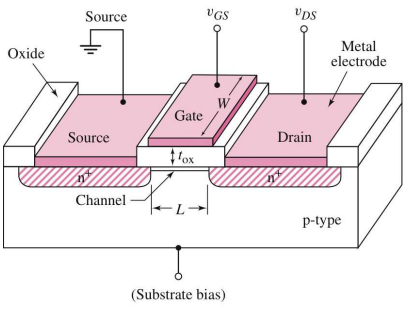
In this chapter, we will:

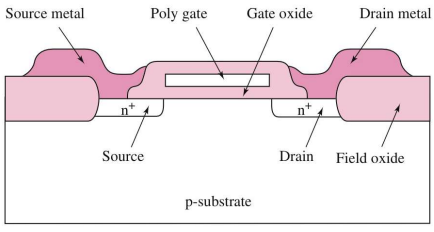
- Study and understand the operation and characteristics of the various types of MOSFETs.
- Understand and become familiar with the dc analysis and design techniques of MOSFET circuits.
- Examine three applications of MOSFET circuits.
- Investigate current source biasing of MOSFET circuits, such as those used in integrated circuits.
- Analyze the dc biasing of multistage or multitransistor circuits.

Basic Structure of MOS Capacitor

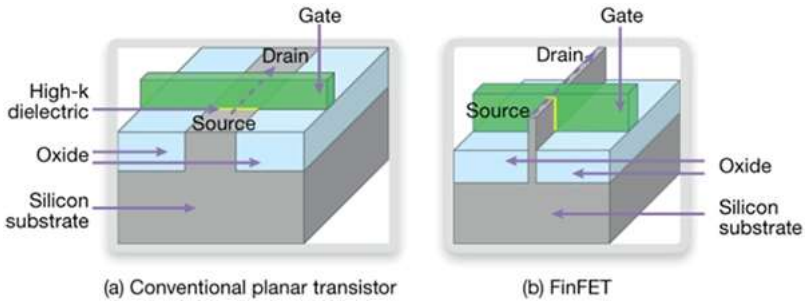


Cross Section of nMOSFET

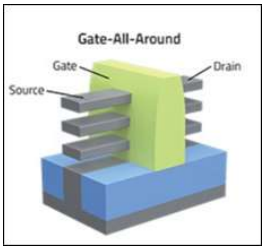




Conventional vs FinFET and Gate-All-Around Structure

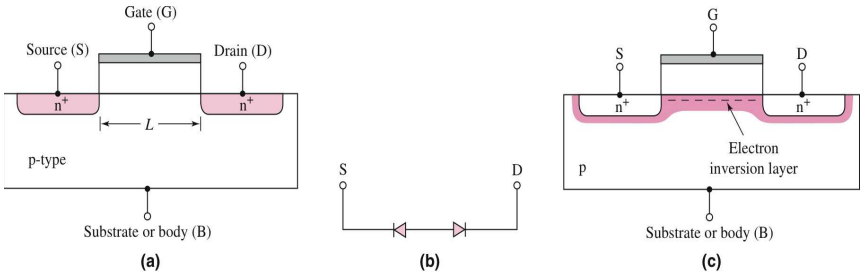


(a) Conventional planar transistor (b) FinFET



(c) Gate-All-Around

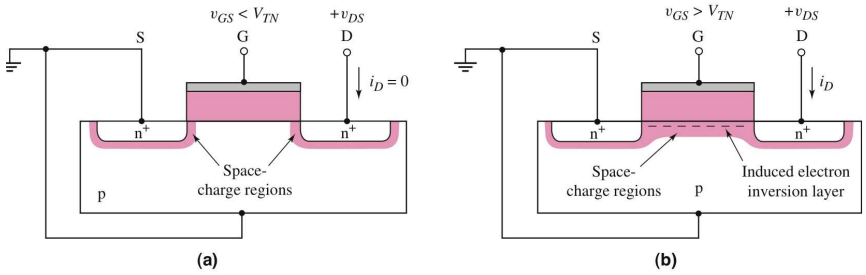
Basic Transistor Operation



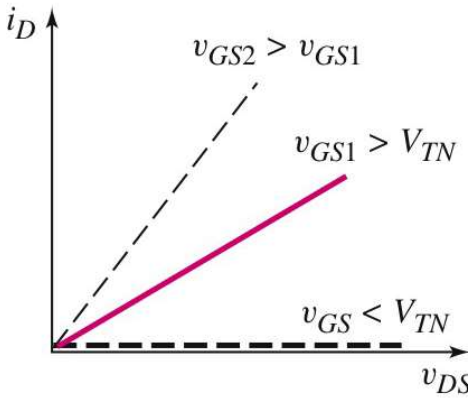
Before electron inversion layer is formed

After electron inversion layer is formed

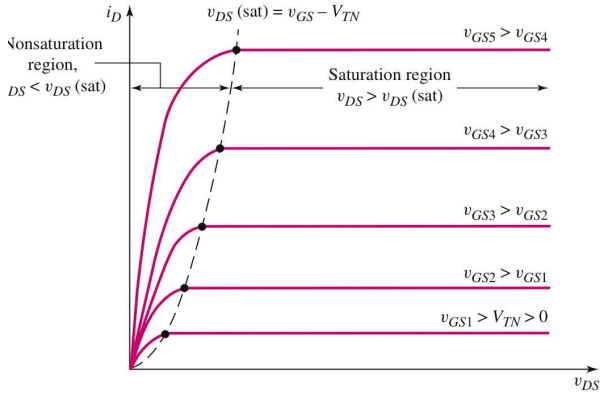
Basic Transistor Operation



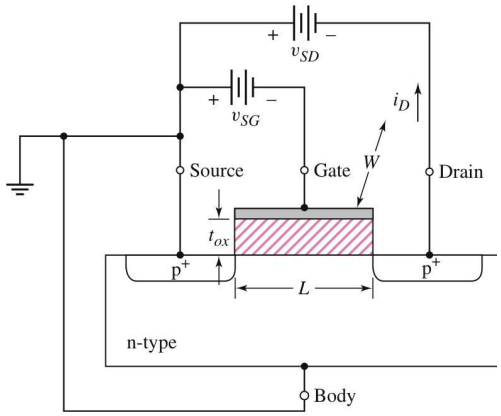
Current Versus Voltage Characteristics: Enhancement-Mode nMOSFET



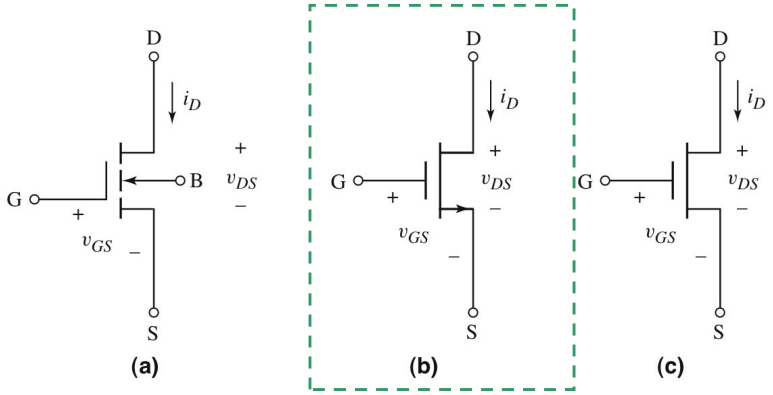
Family of i_D Versus v_{DS} Curves: Enhancement-Mode nMOSFET



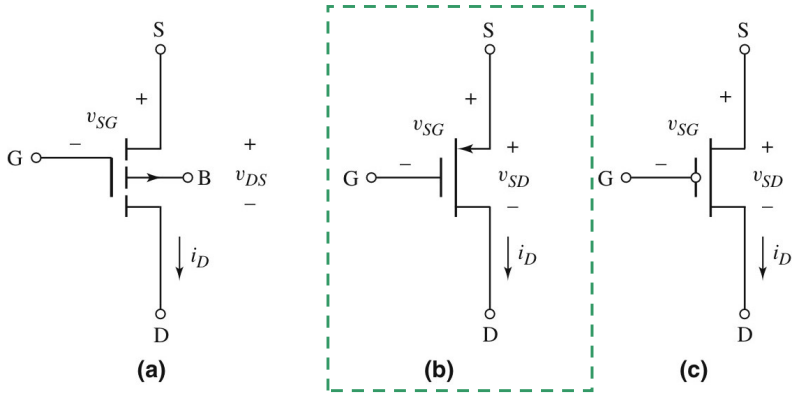
p-Channel Enhancement-Mode MOSFET



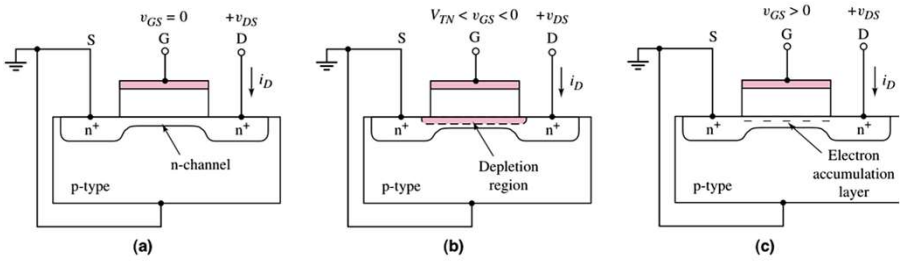
Symbols for n-Channel Enhancement-Mode MOSFET



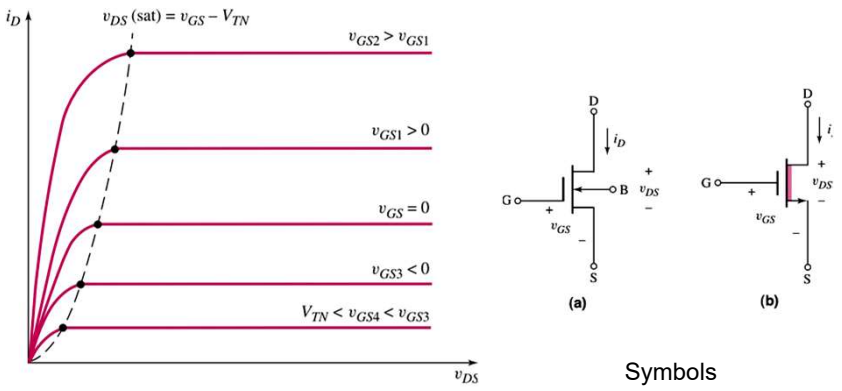
Symbols for p-Channel Enhancement-Mode MOSFET



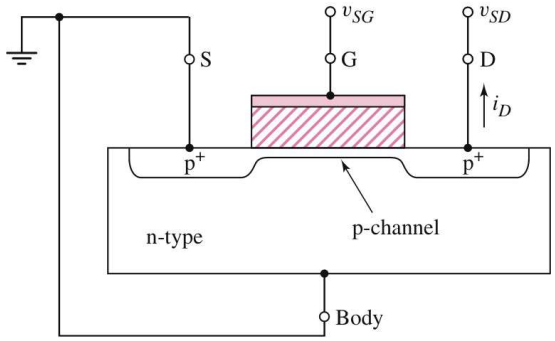
n-Channel Depletion-Mode MOSFET

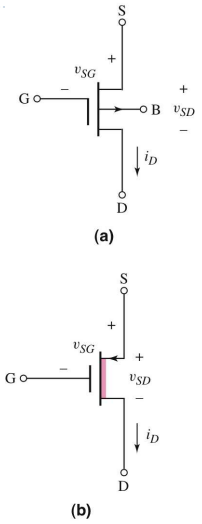


Family of i_D Versus v_{DS} Curves: Depletion-Mode nMOSFET



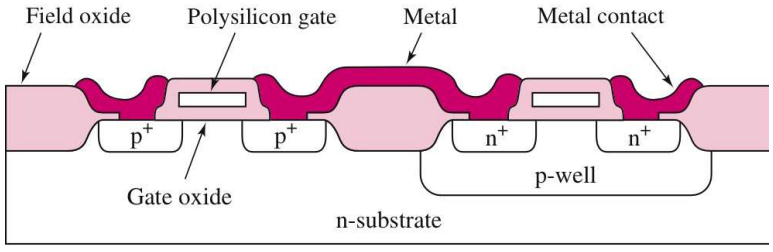
p-Channel Depletion-Mode MOSFET





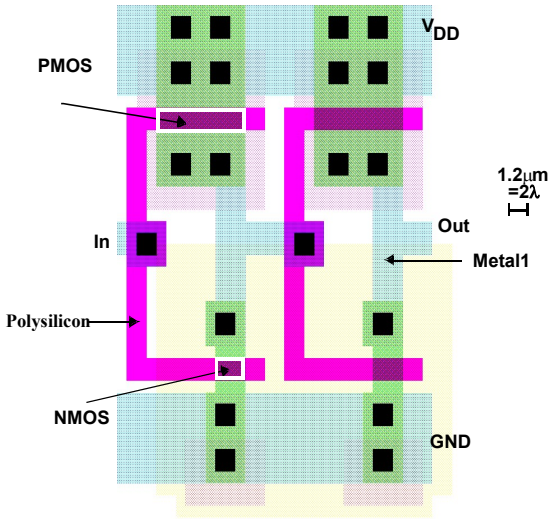
Symbols

Cross-Section of nMOSFET and pMOSFET



Both transistors are used in the fabrication of CMOS circuitry.

CMOS Inverter Layout



Summary of I-V Relationships

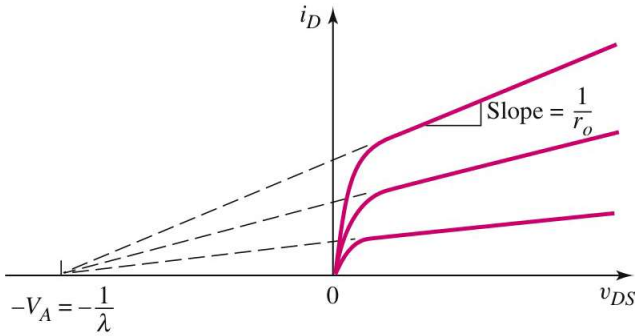
Region	NMOS	PMOS
Nonsaturation	$v_{DS}<v_{DS}(sat)$ $i_D = K_n[2(v_{GS}-V_{TN})v_{DS}-v_{DS}^2]$	$v_{SD}<v_{SD}(sat)$ $i_D = K_p[2(v_{SG}+V_{TP})v_{SD}-v_{SD}^2]$
Saturation	$v_{DS}>v_{DS}(sat)$ $i_D = K_n[v_{GS}-V_{TN}]^2$	$v_{SD}>v_{SD}(sat)$ $i_D = K_p[v_{SG}+V_{TP}]^2$
Transition Pt.	$v_{DS}(sat) = v_{GS} - V_{TN}$	$v_{SD}(sat) = v_{SG} + V_{TN}$
Enhancement Mode	$V_{TN} > 0V$	$V_{TP} < 0V$
Depletion Mode	$V_{TN} < 0V$	$V_{TP} > 0V$

Conduction Parameters

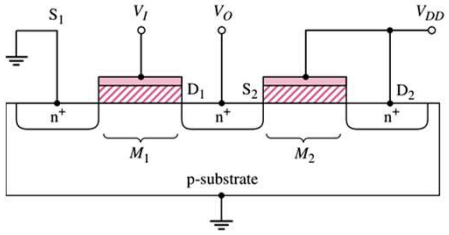
- NMOSFET $K_n = \frac{W\mu_n C_{ox}}{2L} = \frac{k_n' W}{2L}$
- PMOSFET $K_p = \frac{W\mu_p C_{ox}}{2L} = \frac{k_p' W}{2L}$

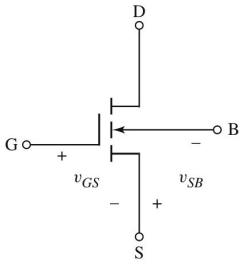
where: $C_{ox} = \varepsilon_o / t_{ox}$

Channel Length Modulation: Early Voltage

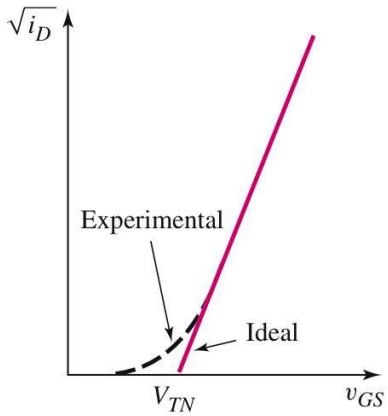


Body Effect

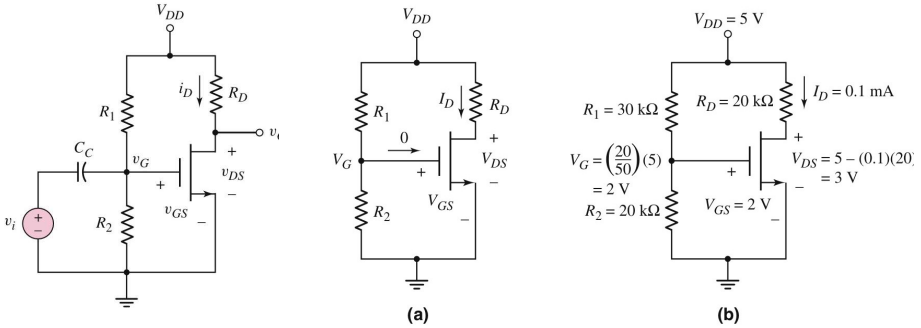




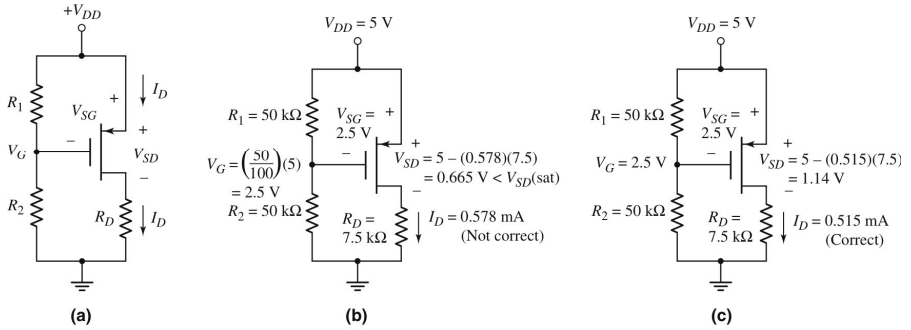
Subthreshold Condition



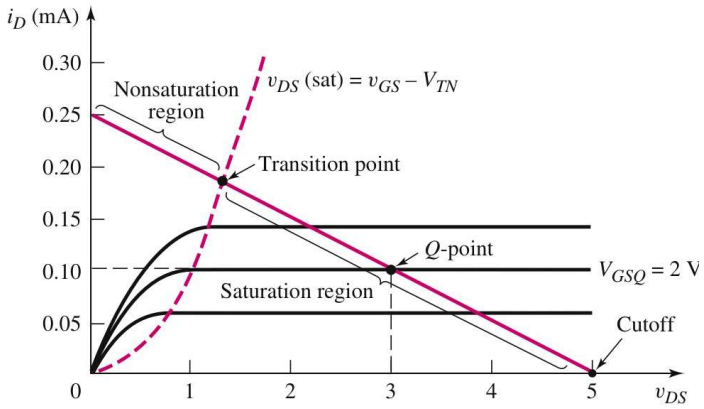
NMOS Common-Source Circuit



PMOS Common-Source Circuit



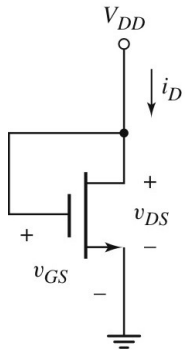
Load Line and Modes of Operation: NMOS Common-Source Circuit

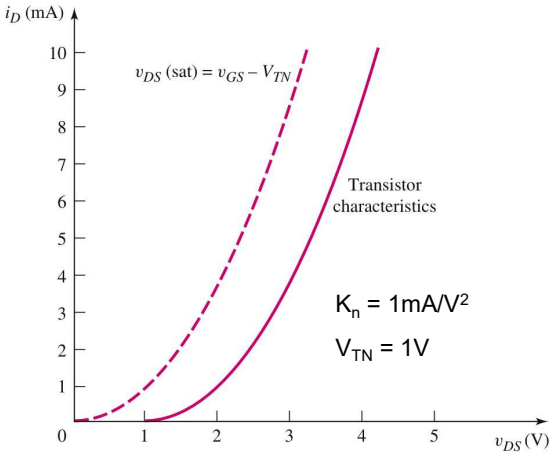


Problem-Solving Technique: NMOSFET DC Analysis

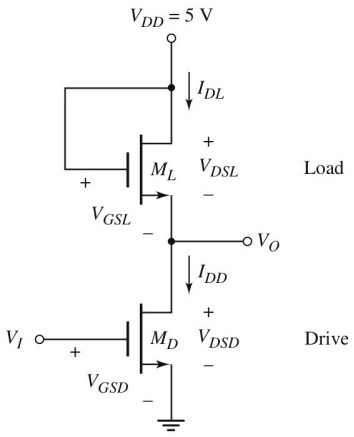
1. Assume the transistor is in saturation.
   a. $V_{GS} > V_{TN}$, $I_D > 0$, & $V_{DS} \geq V_{DS}(sat)$
2. Analyze circuit using saturation I-V relations.
3. Evaluate resulting bias condition of transistor.
   a. If $V_{GS} < V_{TN}$, transistor is likely in cutoff
   b. If $V_{DS} < V_{DS}(sat)$, transistor is likely in nonsaturation region
4. If initial assumption is proven incorrect, make new assumption and repeat Steps 2 and 3.

Enhancement Load Device





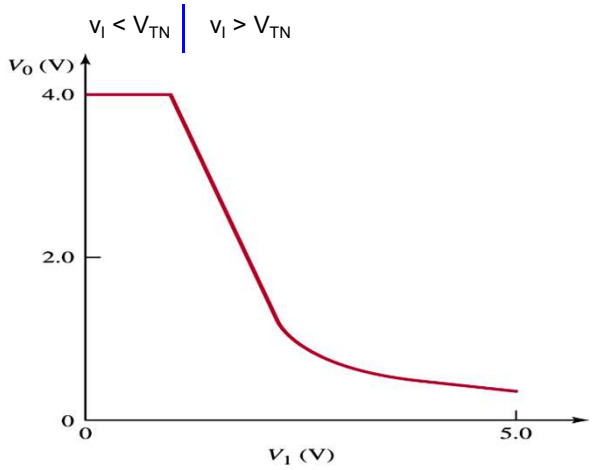
Circuit with Enhancement Load Device and NMOS Driver



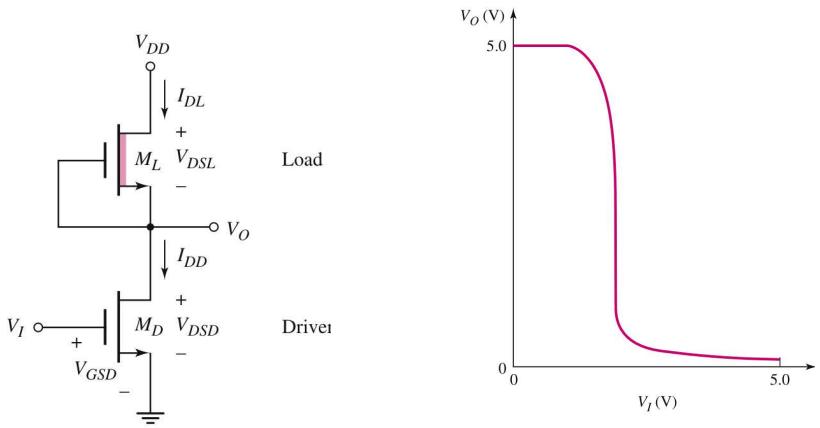
M_L is always in saturation.

M_D can be biased either in saturation or nonsaturation region.

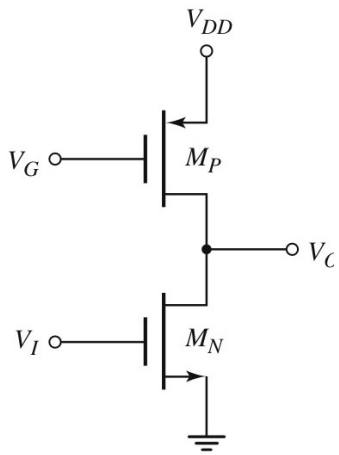
Voltage Transfer Characteristics: NMOS Inverter with Enhancement Load Device

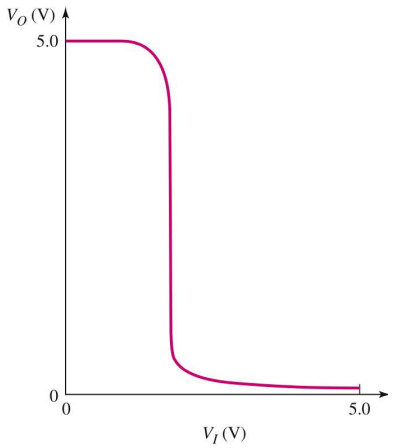


NMOS Inverter with Depletion Load Device

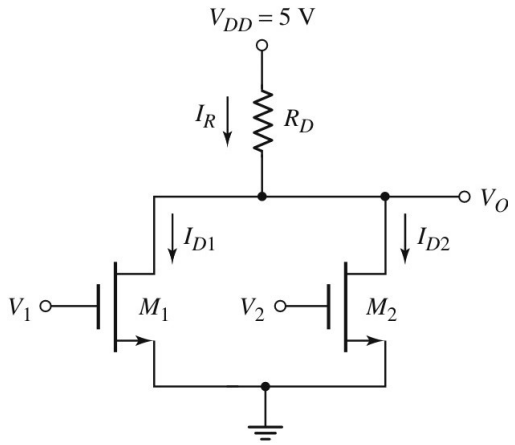


CMOS Inverter



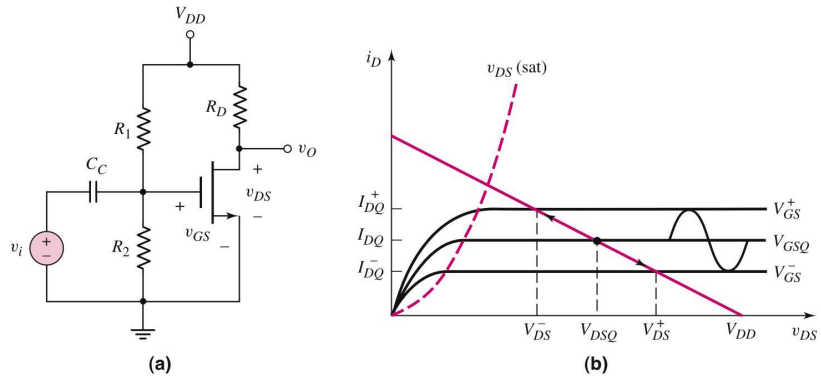


2-Input NMOS NOR Logic Gate

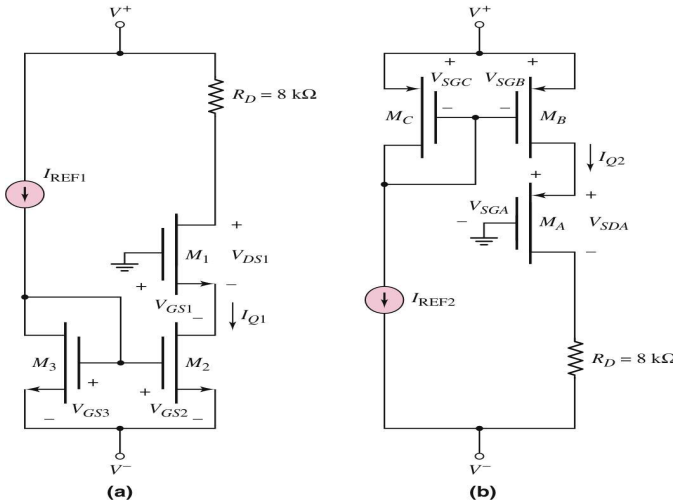


V_1 (V)	V_2 (V)	V_O (V)
0	0	High
5	0	Low
0	5	Low
5	5	Low

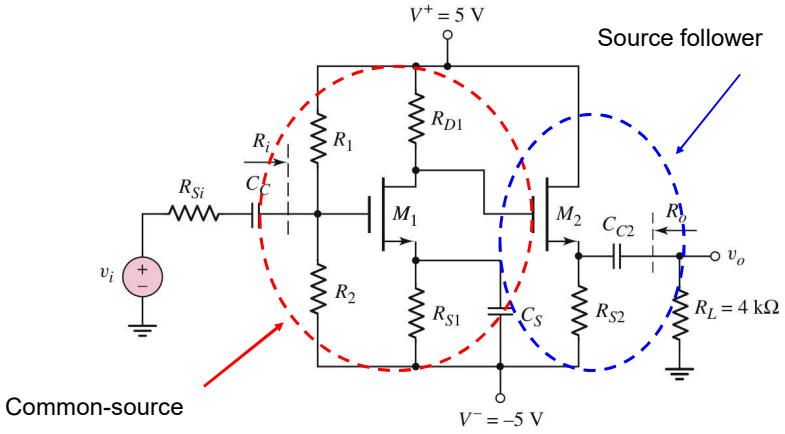
MOS Small-Signal Amplifier



Current Mirrors



2-Stage Cascade Amplifier



NMOS Cascode Circuit