Microelectronics
Circuit Analysis and Design

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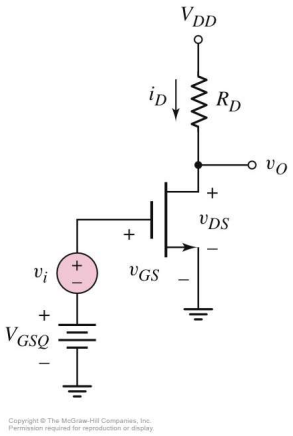
Chapter 4

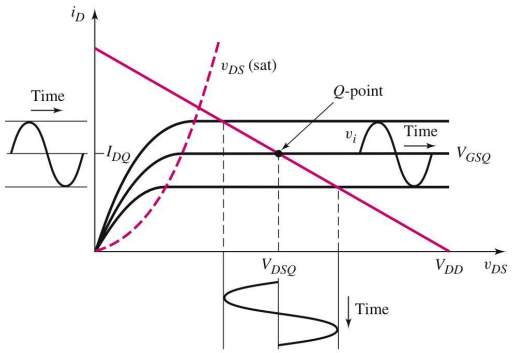
Basic FET Amplifiers

In this chapter, we will:

- Investigate a single-transistor circuit that can amplify a small, time-varying input signal
  - Develop small-signal models that are used in the analysis of linear amplifiers.
- Discuss and compare the three basic transistor amplifier configurations.
  - Analyze the common-source amplifier.
  - Analyze the source-follower amplifier.
  - Analyze the common-gate amplifier.
- Analyze multitransistor or multistage amplifiers.
- Develop the small-signal model of JFET devices and analyze basic JFET amplifiers.
- Design a two-stage MOSFET amplifier circuit.

NMOS Common-Source Circuit





NMOS Transistor Small-Signal Parameters

- Values depends on Q-point

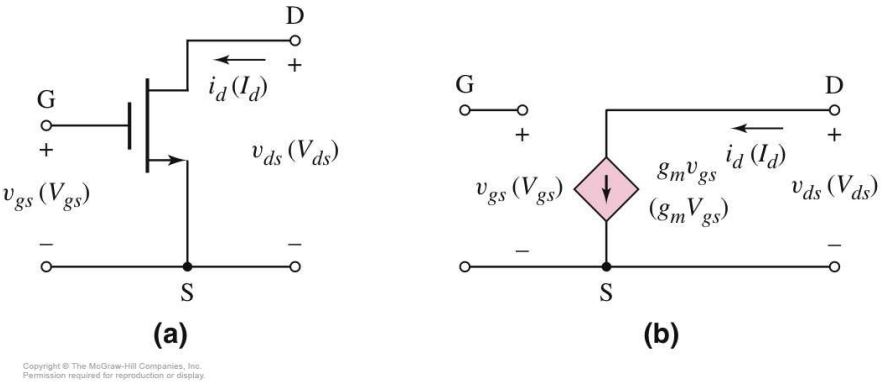
$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{i_d}{v_{gs}}$$

$$g_m = 2K_n(V_{GSQ} - V_{TN}) = 2\sqrt{K_n I_{DQ}}$$

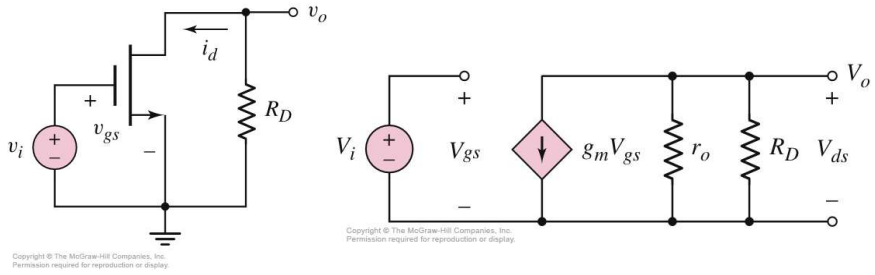
$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}}\right)^{-1}$$

$$r_o = [\lambda K_n (V_{GSQ} - V_{TN})^2]^{-1} \cong [\lambda I_{DQ}]^{-1}$$

Simple NMOS Small-Signal Equivalent Circuit



NMOS Common-Source Circuit



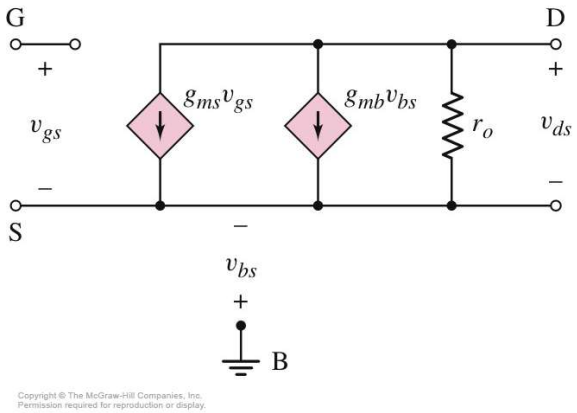
AC Small-signal

$$A_v = V_o / V_i = -g_m (r_o \| R_D)$$

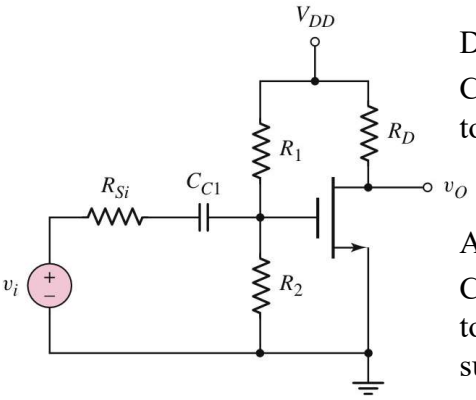
Problem-Solving Technique: MOSFET AC Analysis

1. Analyze circuit with only the dc sources to find quiescent solution. Transistor must be biased in saturation region for linear amplifier.
2. Replace elements with small-signal model.
3. Analyze small-signal equivalent circuit, setting dc sources to zero, to produce the circuit to the time-varying input signals only.

Modeling the Body Effects



Common-Source Configuration



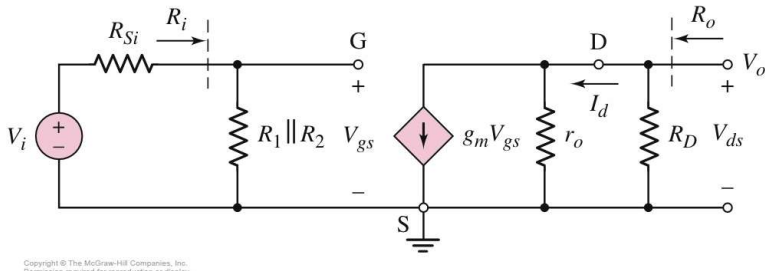
DC analysis:

Coupling capacitor is assumed to be open.

AC analysis:

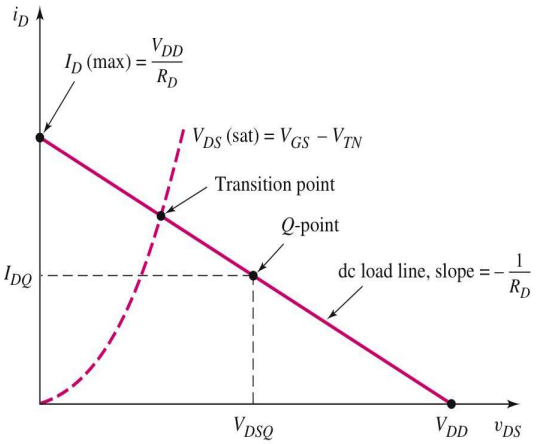
Coupling capacitor is assumed to be a short. DC voltage supply is set to zero volts.

Small-Signal Equivalent Circuit



$$A_v = V_o / V_i = -g_m (r_o \| R_D)\left(\frac{R_i}{R_i + R_{Si}}\right)$$

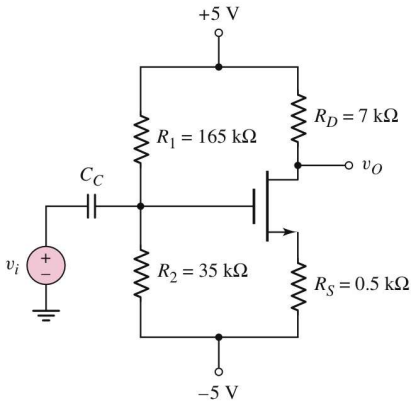
DC Load Line



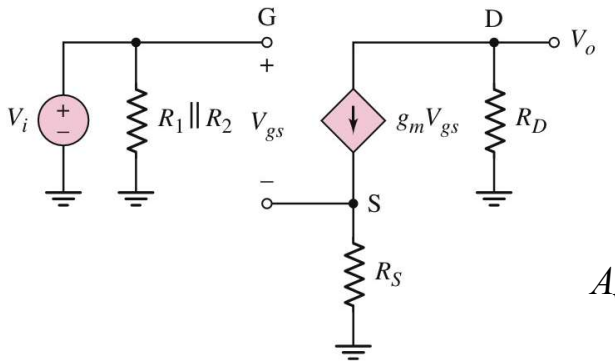
Q-point near the middle of the saturation region for maximum symmetrical output voltage swing,.

Small AC input signal for output response to be linear.

Common-Source Amplifier with Source Resistor

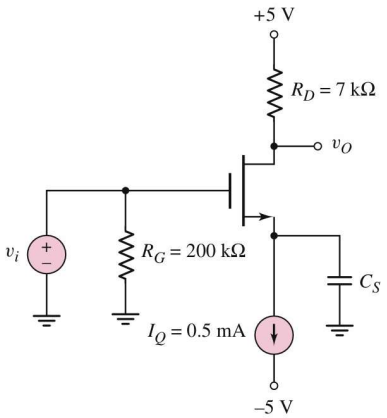


Small-Signal Equivalent Circuit for Common-Source with Source Resistor

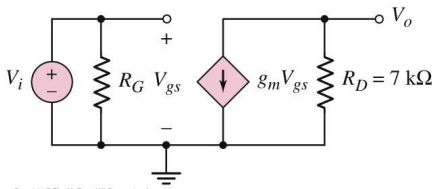


$$A_v = \frac{-g_m R_D}{1 + g_m R_S}$$

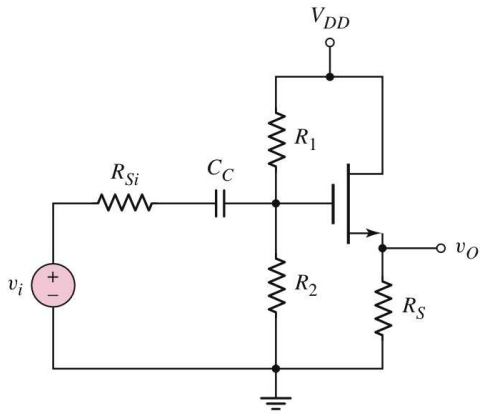
Common-Source Amplifier with Bypass Capacitor



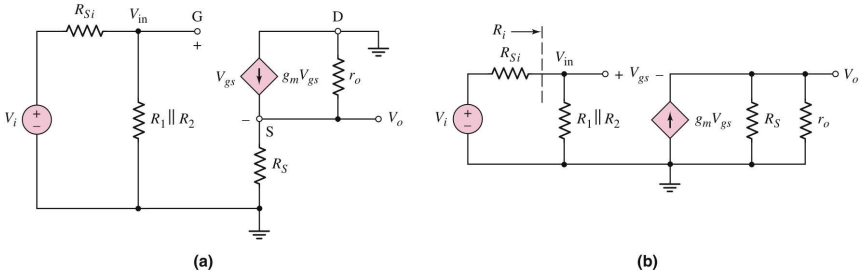
Small-signal equivalent circuit



NMOS Source-Follower or Common Drain Amplifier

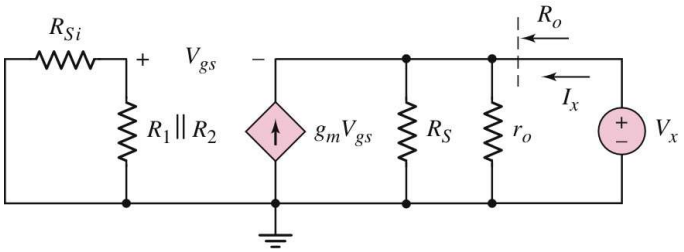


Small-Signal Equivalent Circuit for Source Follower



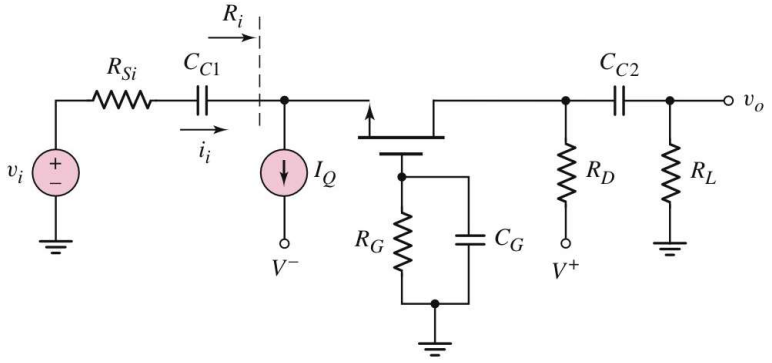
$$A_v = \frac{R_S \| r_o}{\frac{1}{g_m} + R_S \| r_o} \left(\frac{R_i}{R_i + R_{Si}} \right)$$

Determining Output Impedance NMOS Source Follower

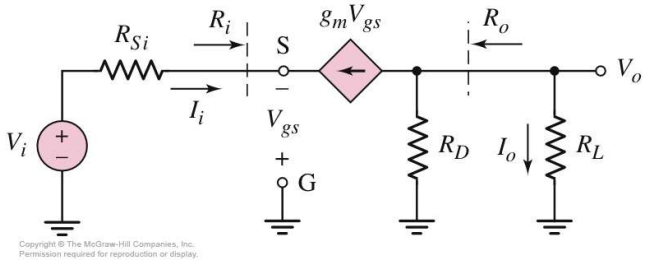


$$R_O = \frac{1}{g_m} \Big\| R_S \| r_o$$

Common-Gate Circuit



Small-Signal Equivalent Circuit for Common Gate

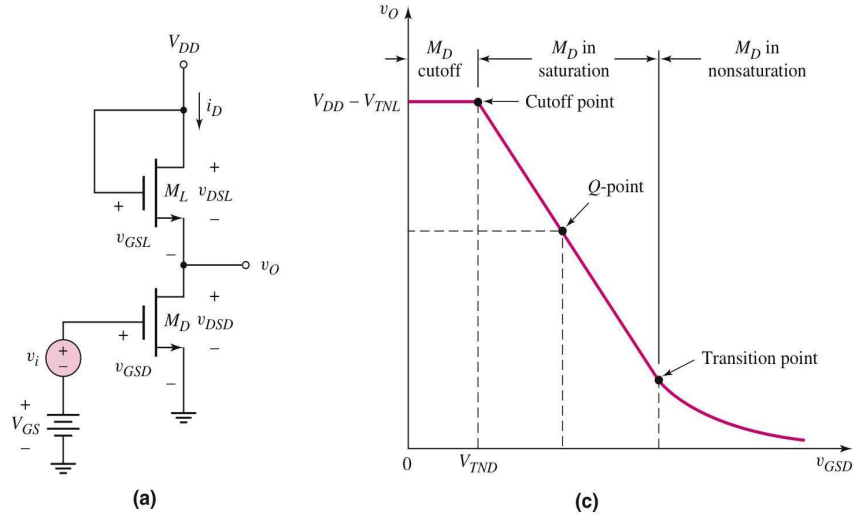


$$A_v = \frac{g_m (R_D \| R_L)}{1 + g_m R_{Si}} \qquad A_i = \frac{I_O}{I_i} = \left(\frac{R_D}{R_D + R_L}\right)\left(\frac{g_m R_{Si}}{1 + g_m R_{Si}}\right)$$

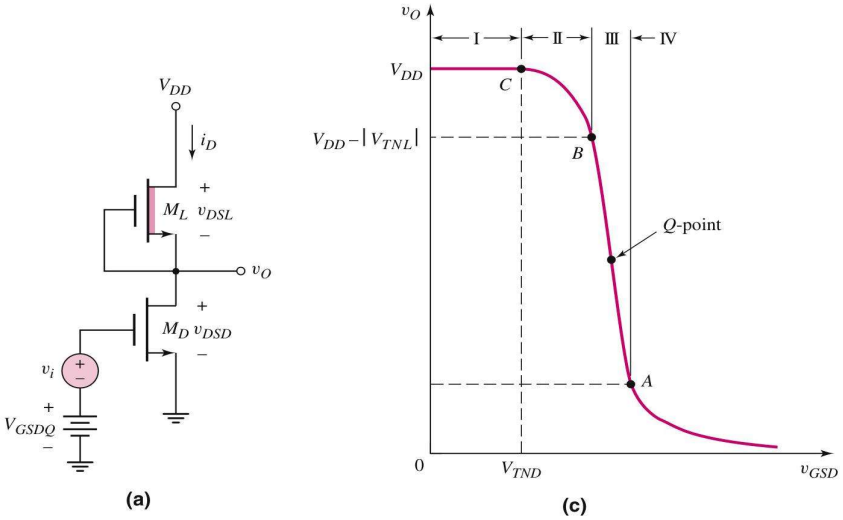
Comparison of 3 Basic Amplifiers

Configuration	Voltage Gain	Current Gain	Input Resistance	Output Resistance
Common Source	$A_v > 1$	—	R_{TH}	Moderate to high
Source Follower	$A_v \approx 1$	—	R_{TH}	Low
Common Gate	$A_v > 1$	$A_i \approx 1$	Low	Moderate to high

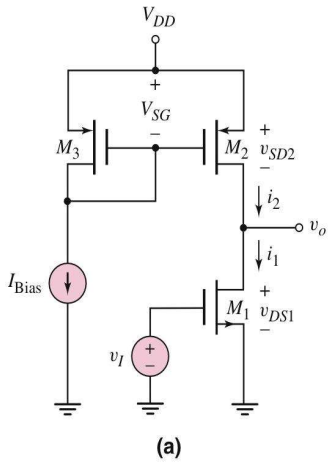
NMOS Amplifier with Enhancement Load Device



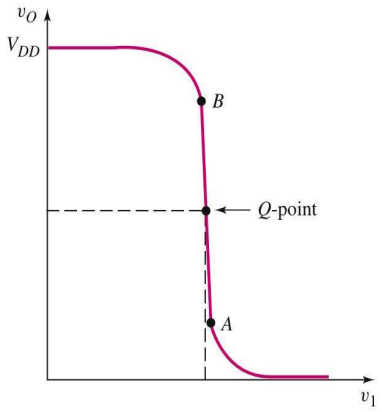
NMOS Amplifier with Depletion Load Device



CMOS Common-Source Amplifier

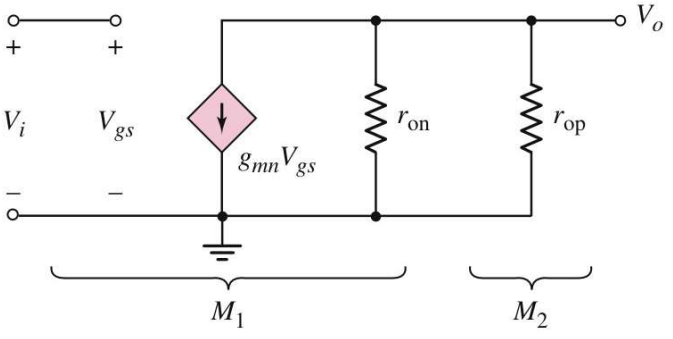


(a)



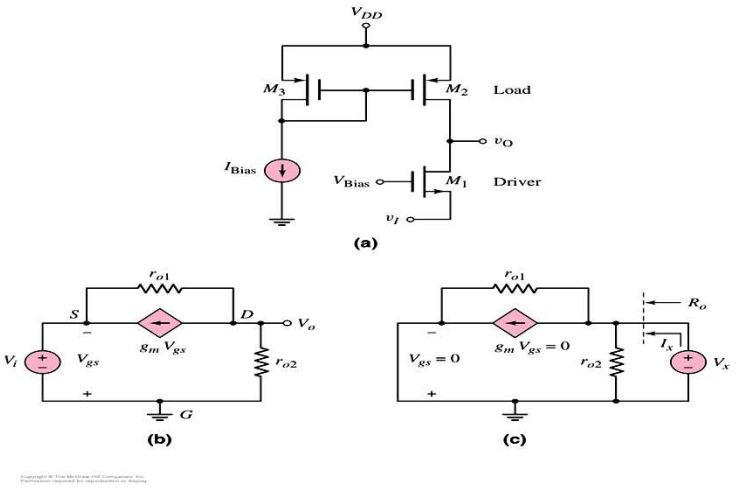
(d)

Small-Signal Equivalent Circuit for CMOS Common Source

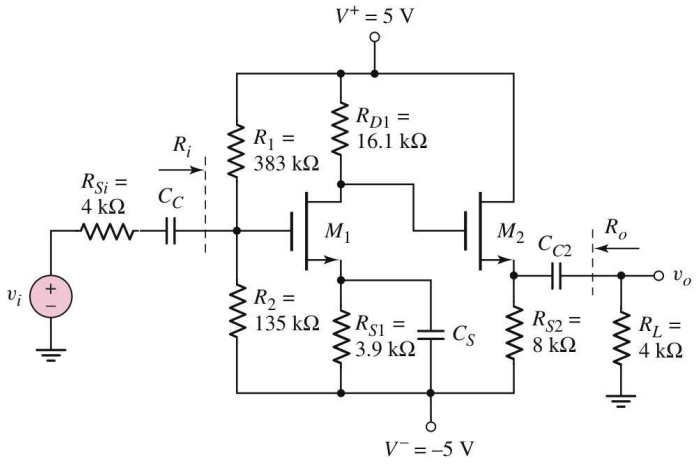


$$A_v = -g_{mn}(r_{on} \| r_{op})$$

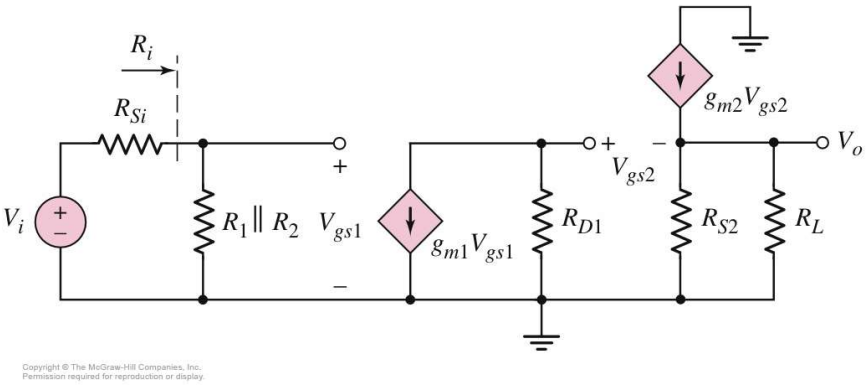
CMOS Common Gate



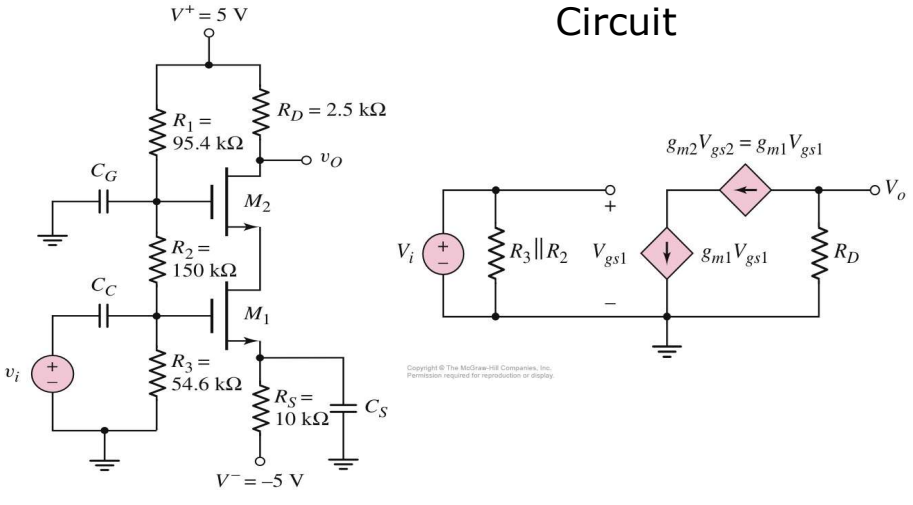
Cascade Circuit



Small-Signal Equivalent Circuit for Cascade Circuit



Cascode Circuit th Small-Signal Equivalent Circuit



JFET Common-Source Amplifier with Small-Signal Equivalent Circuit