

Microelectronics Circuit Analysis and Design

Donald A. Neamen

Chapter 3

The Field Effect Transistor

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Chapter 3-1

In this chapter, we will:

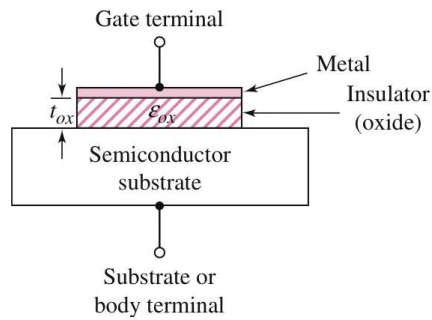
- Study and understand the operation and characteristics of the various types of MOSFETs.
- Understand and become familiar with the dc analysis and design techniques of MOSFET circuits.
- Examine three applications of MOSFET circuits.
- Investigate current source biasing of MOSFET circuits, such as those used in integrated circuits.
- Analyze the dc biasing of multistage or multitransistor circuits.
- Understand the operation and characteristics of the junction field-effect transistor, and analyze the dc response of JFET circuits.

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Basic Structure of MOS Capacitor



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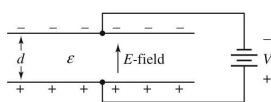
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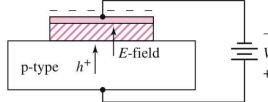
MOS Capacitor Under Bias: Electric Field and Charge

Parallel plate capacitor



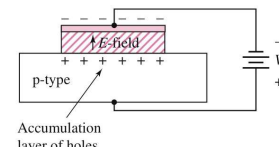
(a)

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(b)

Negative gate bias:
Holes attracted to gate



(c)

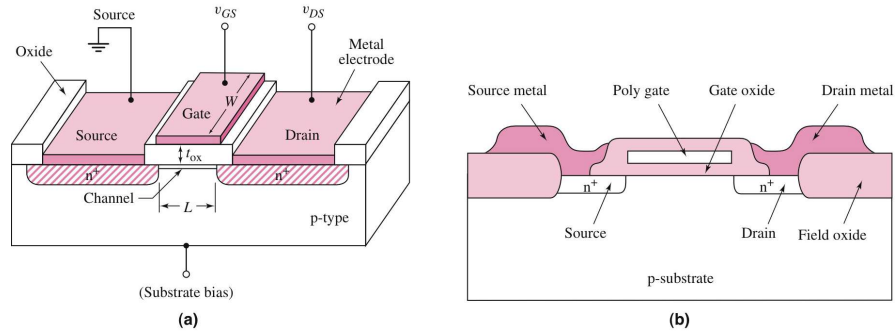
Positive gate bias:
Electrons attracted to gate

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Schematic of n-Channel Enhancement Mode MOSFET

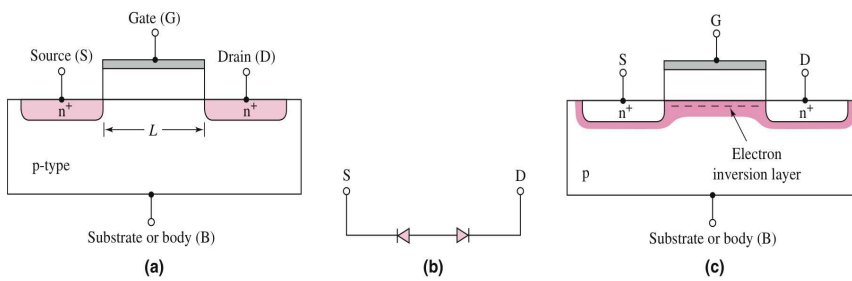


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Basic Transistor Operation



Before electron
inversion layer is
formed

After electron
inversion layer is
formed

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Basic Transistor Operation

(a) $v_{GS} < V_{TN}$, $i_D = 0$

(b) $v_{GS} > V_{TN}$, i_D

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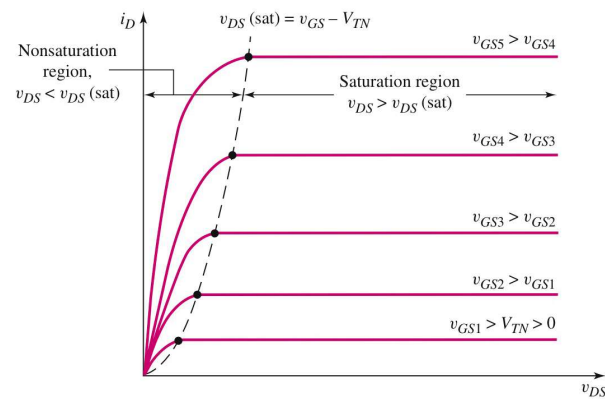
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Current Versus Voltage Characteristics: Enhancement-Mode nMOSFET

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Family of i_D Versus v_{DS} Curves: Enhancement-Mode nMOSFET

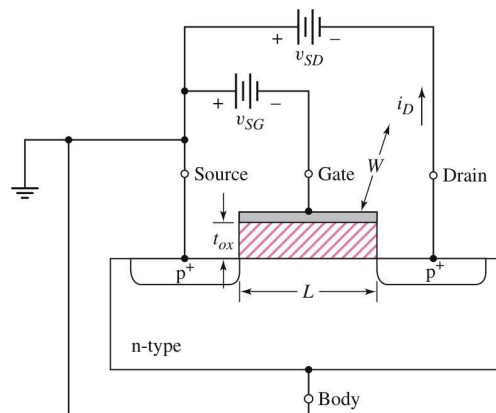


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p-Channel Enhancement-Mode MOSFET



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Symbols for n-Channel Enhancement-Mode MOSFET

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Symbols for p-Channel Enhancement-Mode MOSFET

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n-Channel Depletion-Mode MOSFET

(a) (b) (c)

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Family of i_D Versus v_{DS} Curves: Depletion-Mode nMOSFET

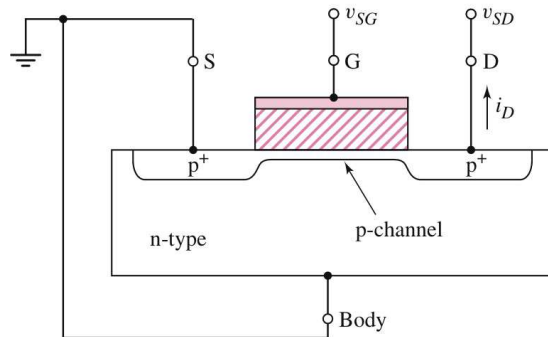
(a) (b)

Symbols

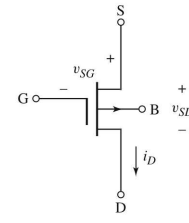
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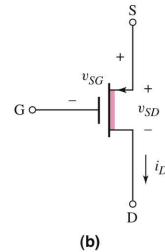
p-Channel Depletion-Mode MOSFET



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(a)



(b)

Symbols

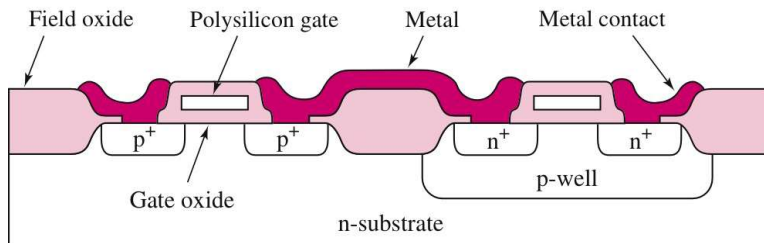
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Cross-Section of nMOSFET and pMOSFET



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Both transistors are used in the fabrication of CMOS circuitry.

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Summary of I-V Relationships

Region	NMOS	PMOS
Nonsaturation	$v_{DS} < v_{DS}(\text{sat})$ $i_D = K_n [2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2]$	$v_{SD} < v_{SD}(\text{sat})$ $i_D = K_p [2(v_{SG} + V_{TP})v_{SD} - v_{SD}^2]$
Saturation	$v_{DS} > v_{DS}(\text{sat})$ $i_D = K_n [v_{GS} - V_{TN}]^2$	$v_{SD} > v_{SD}(\text{sat})$ $i_D = K_p [v_{SG} + V_{TP}]^2$
Transition Pt.	$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$
Enhancement Mode	$V_{TN} > 0V$	$V_{TP} < 0V$
Depletion Mode	$V_{TN} < 0V$	$V_{TP} > 0V$

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Conduction Parameters

□ NMOSFET
$$K_n = \frac{W\mu_n C_{ox}}{L} = k'_n \frac{W}{L}$$

□ PMOSFET
$$K_p = \frac{W\mu_p C_{ox}}{L} = k'_p \frac{W}{L}$$

where:

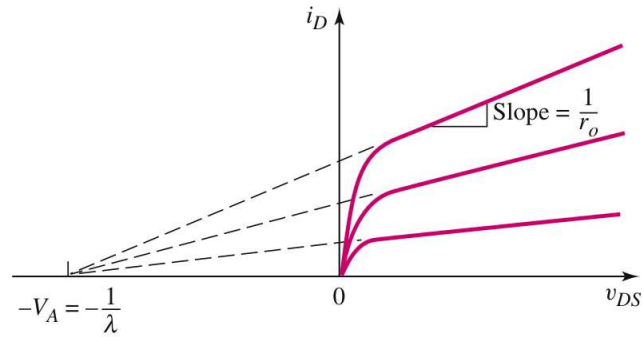
$$C_{ox} = \epsilon_o / t_{ox}$$

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Channel Length Modulation: Early Voltage



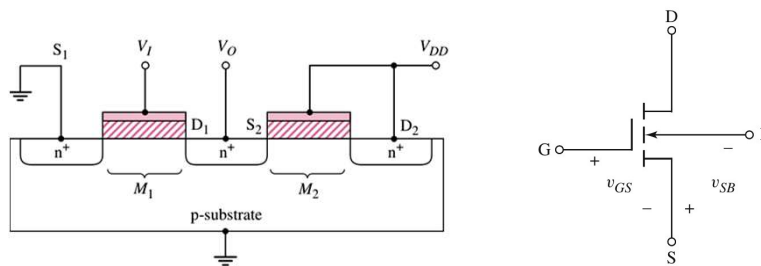
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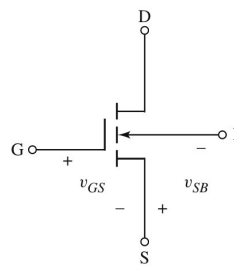
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Body Effect



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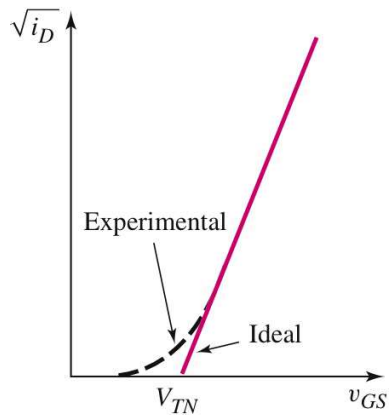
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Subthreshold Condition



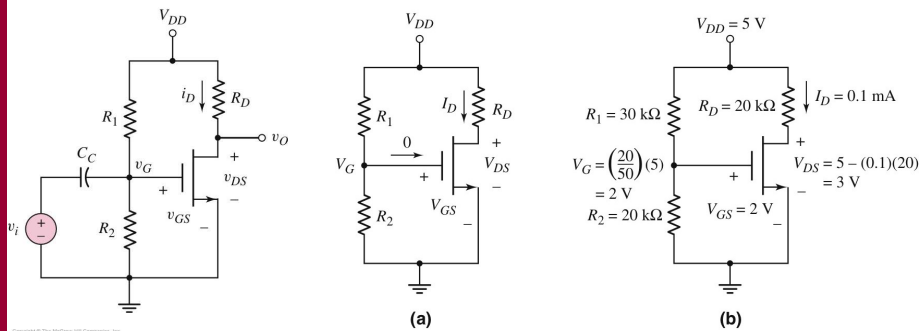
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NMOS Common-Source Circuit



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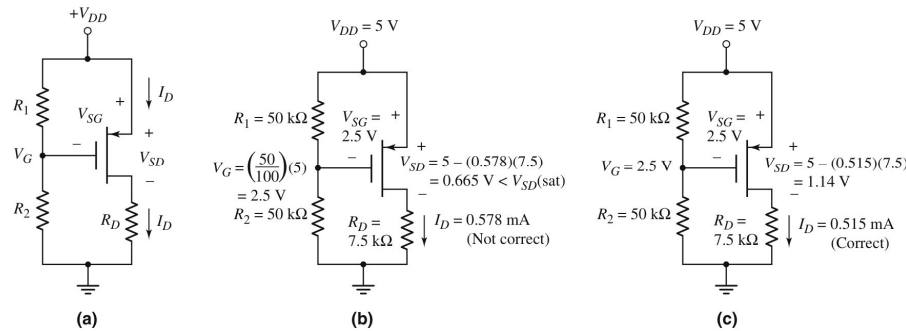
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PMOS Common-Source Circuit

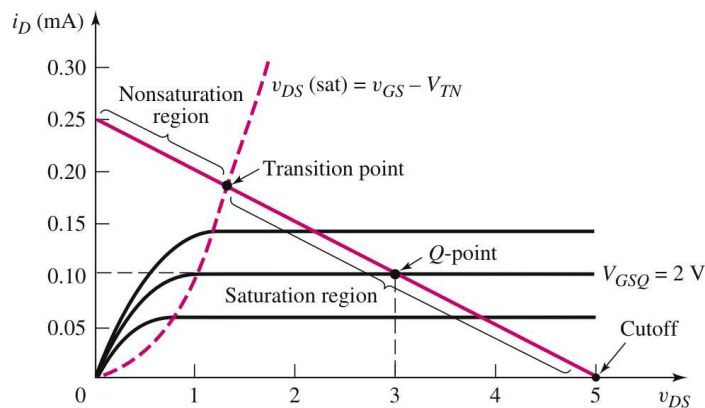


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Load Line and Modes of Operation: NMOS Common-Source Circuit



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Problem-Solving Technique: NMOSFET DC Analysis

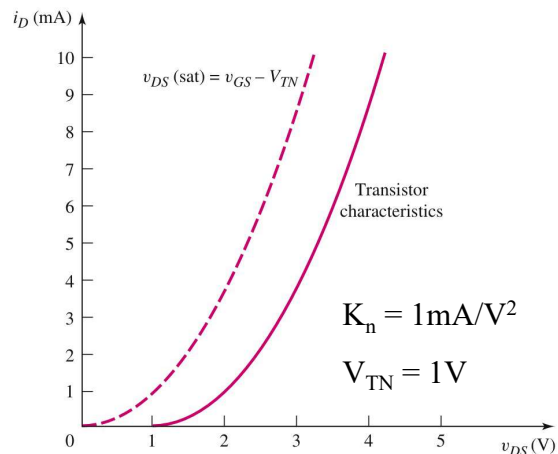
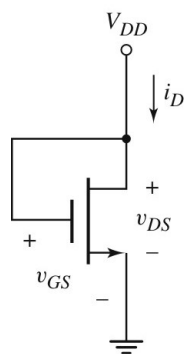
1. Assume the transistor is in saturation.
 - a. $V_{GS} > V_{TN}$, $I_D > 0$, & $V_{DS} \geq V_{DS}(\text{sat})$
2. Analyze circuit using saturation I-V relations.
3. Evaluate resulting bias condition of transistor.
 - a. If $V_{GS} < V_{TN}$, transistor is likely in cutoff
 - b. If $V_{DS} < V_{DS}(\text{sat})$, transistor is likely in nonsaturation region
4. If initial assumption is proven incorrect, make new assumption and repeat Steps 2 and 3.

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Enhancement Load Device



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Circuit with Enhancement Load Device and NMOS Driver

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M_L is always in saturation.

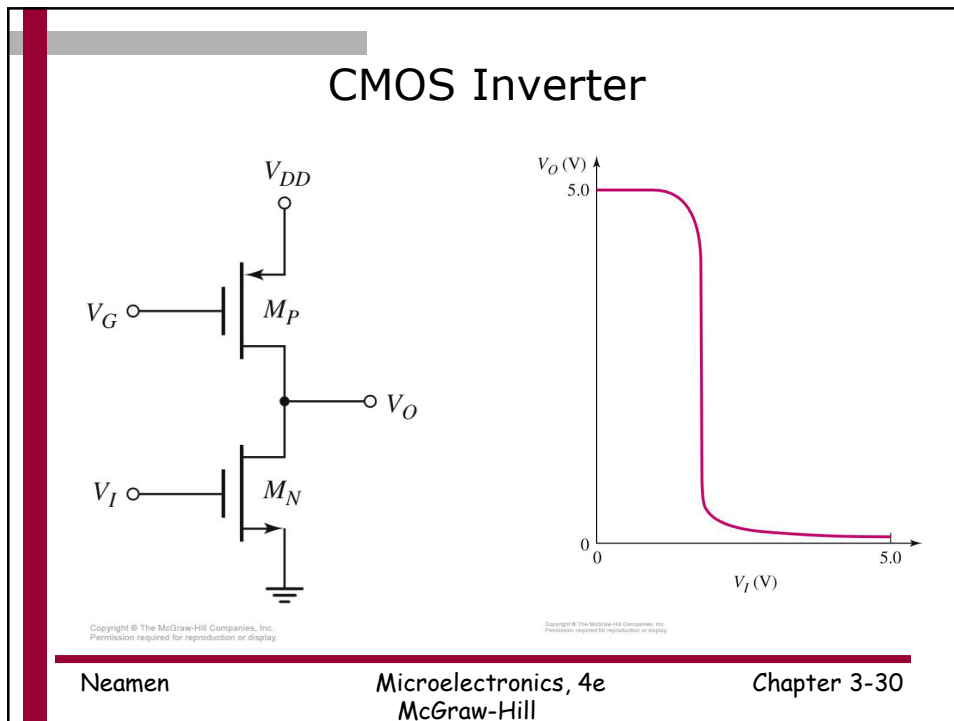
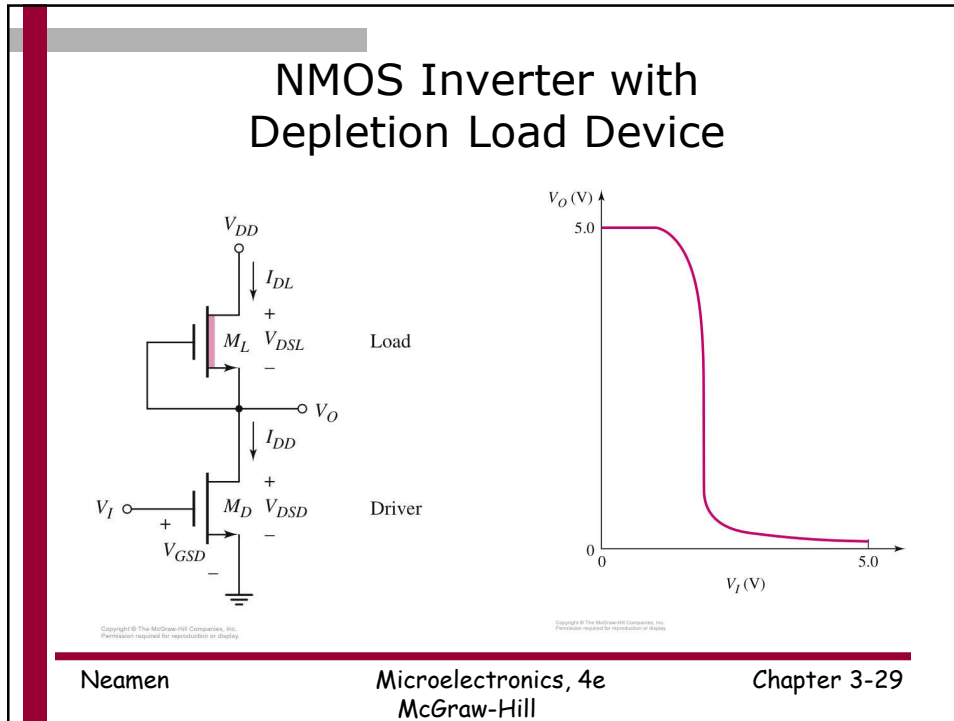
M_D can be biased either in saturation or nonsaturation region.

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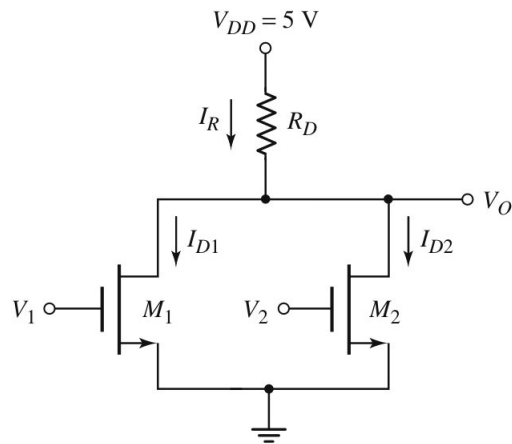
Voltage Transfer Characteristics: NMOS Inverter with Enhancement Load Device

$v_I < V_{TN} \quad | \quad v_I > V_{TN}$

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2-Input NMOS NOR Logic Gate



V_1 (V)	V_2 (V)	V_O (V)
0	0	High
5	0	Low
0	5	Low
5	5	Low

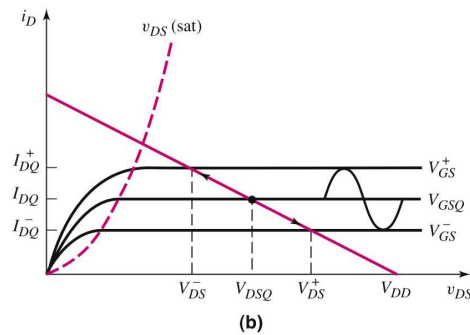
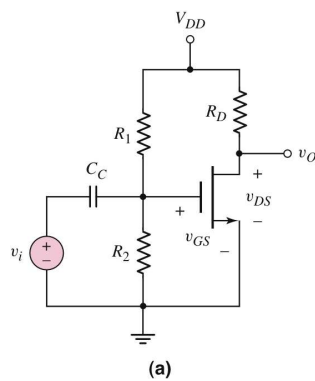
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MOS Small-Signal Amplifier



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Current Mirrors

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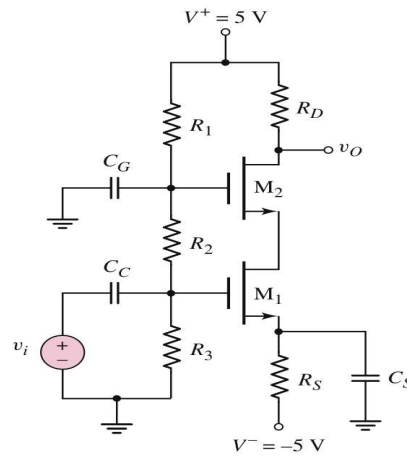
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2-Stage Cascade Amplifier

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NMOS Cascode Circuit



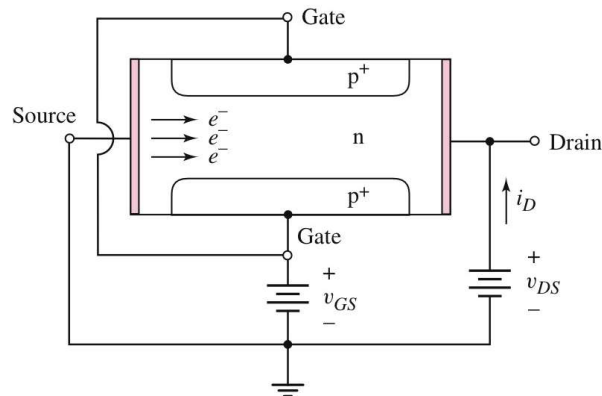
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Cross Section of n-Channel Junction Field Effect Transistor (JFET)



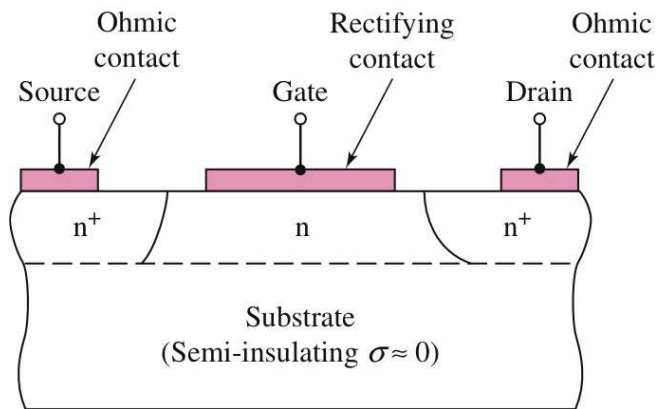
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Cross Section of n-Channel MESFET



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