Laboratorij za načrtovanje integriranih vezij

FE UNIVERZA V LJUBLJANI
Fakulteta za elektrotehniko

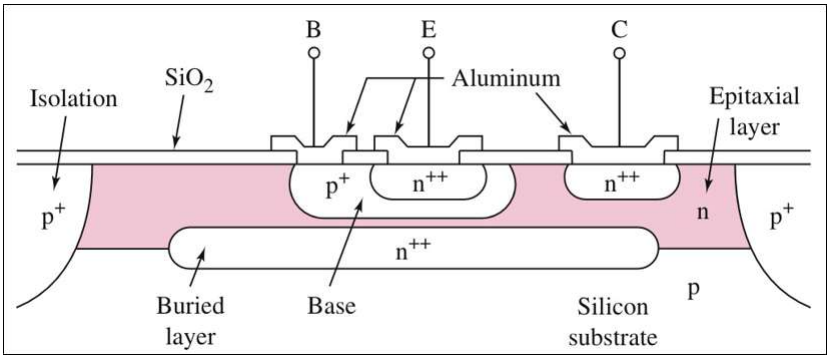
Linearna elektronska vezja

Bipolarni tranzistor

In this chapter, we will:

- Discuss the physical structure and operation of the bipolar junction transistor.
- Understand the dc analysis and design techniques of bipolar transistor circuits.
- Examine three basic applications of bipolar transistor circuits.
- Investigate various dc biasing schemes of bipolar transistor circuits, including integrated circuit biasing.
- Consider the dc biasing of multistage or multi-transistor circuits.

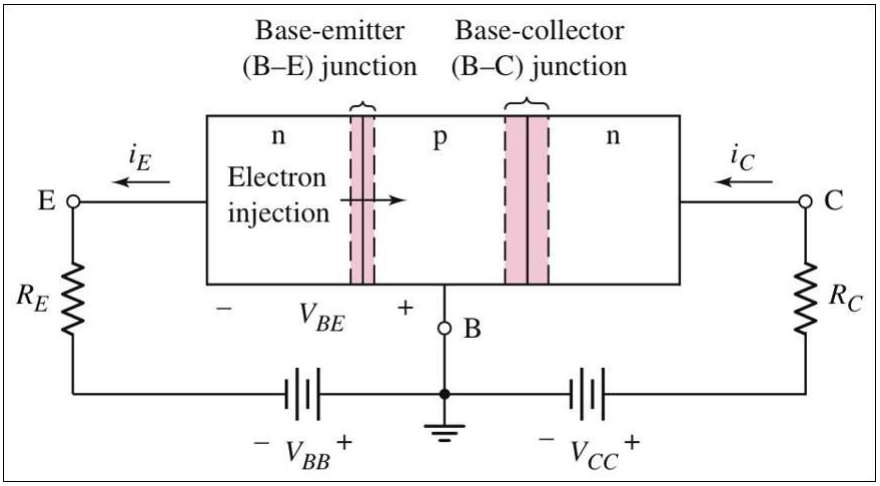
Cross Section of Integrated Circuit npn Transistor



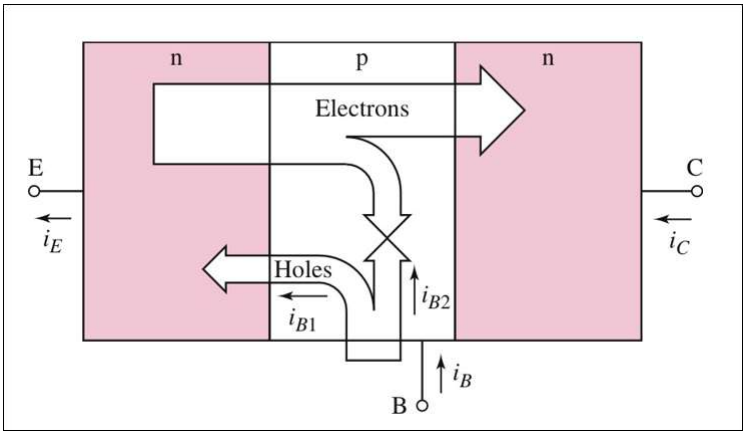
Modes of Operation

- Forward-Active
  - B-E junction is forward biased
  - B-C junction is reverse biased
- Saturation
  - B-E and B-C junctions are forward biased
- Cut-Off
  - B-E and B-C junctions are reverse biased
- Inverse-Active (or Reverse-Active)
  - B-E junction is reverse biased
  - B-C junction is forward biased

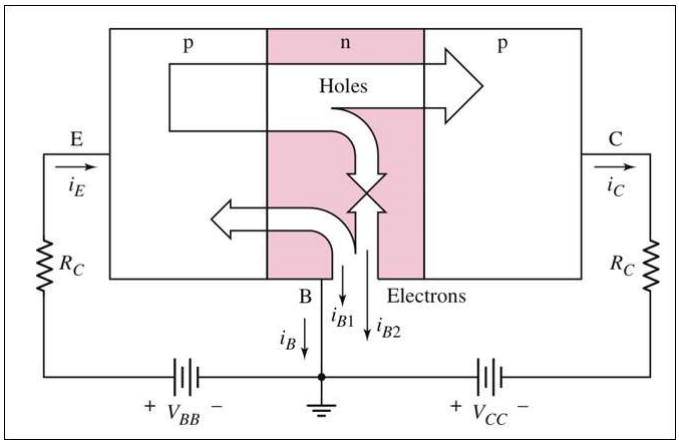
npn BT in Forward-Active



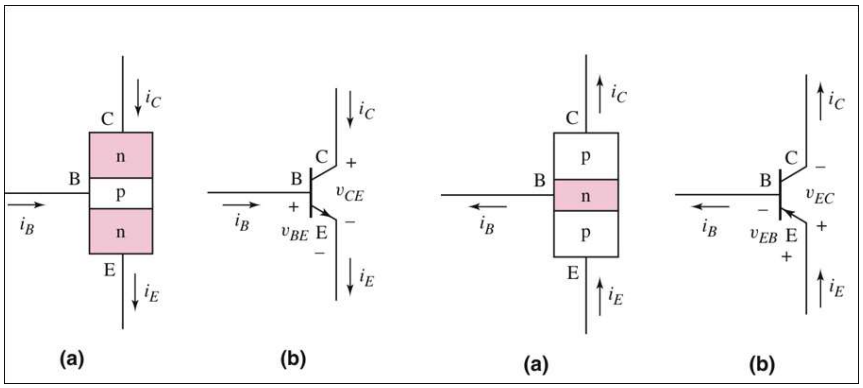
Electrons and Holes in npn BT



Electrons and Holes in pnp BJT



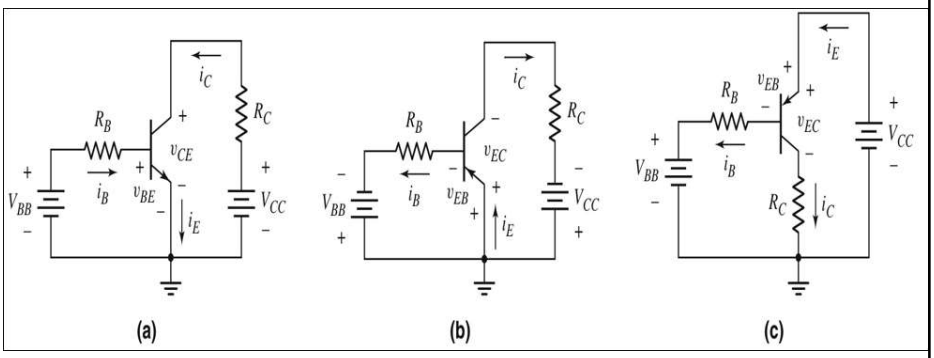
Circuit Symbols and Current Conventions



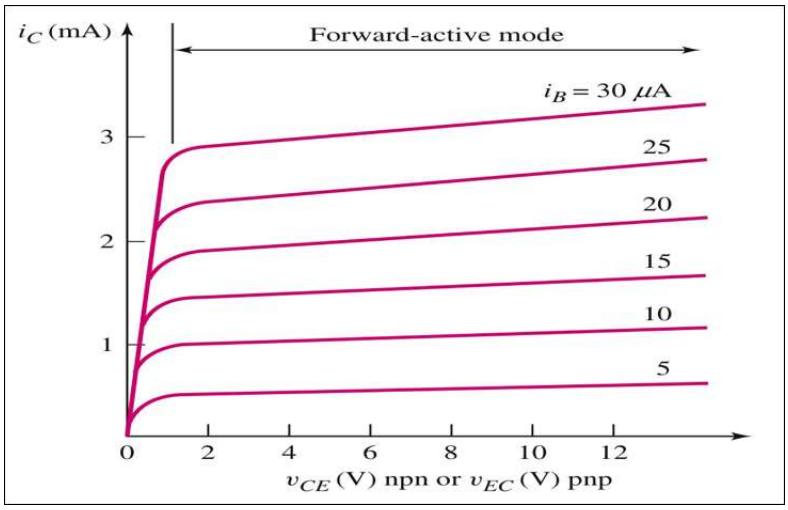
Current Relationships

$$i_E = i_C + i_B$$
$$i_C = \beta i_B$$
$$i_E = (1+\beta) i_B$$
$$i_C = \alpha i_E$$
$$\beta = \frac{\alpha}{1-\alpha}$$

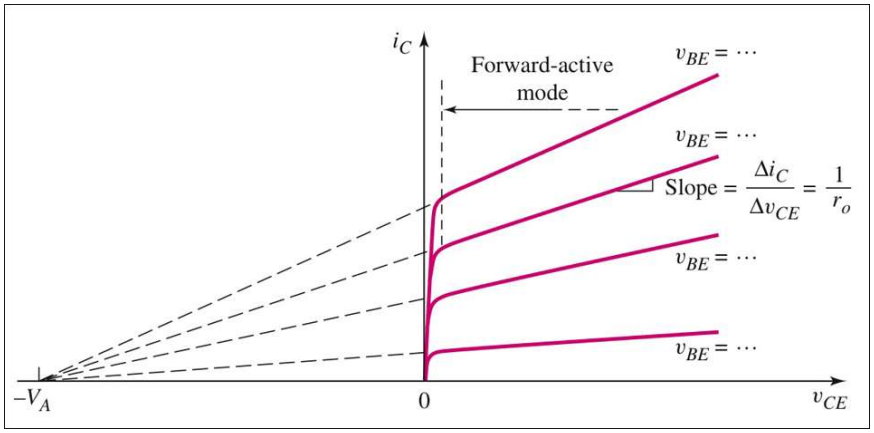
Common-Emitter Configurations



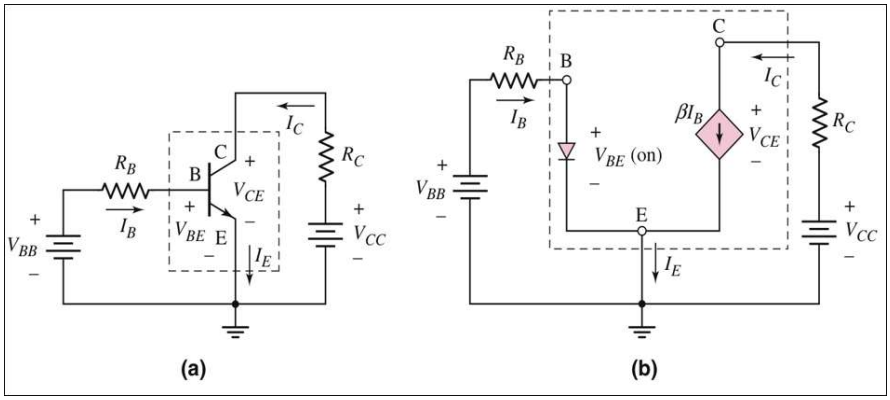
Current-Voltage Characteristics of a Common-Emitter (C-E) Circuit



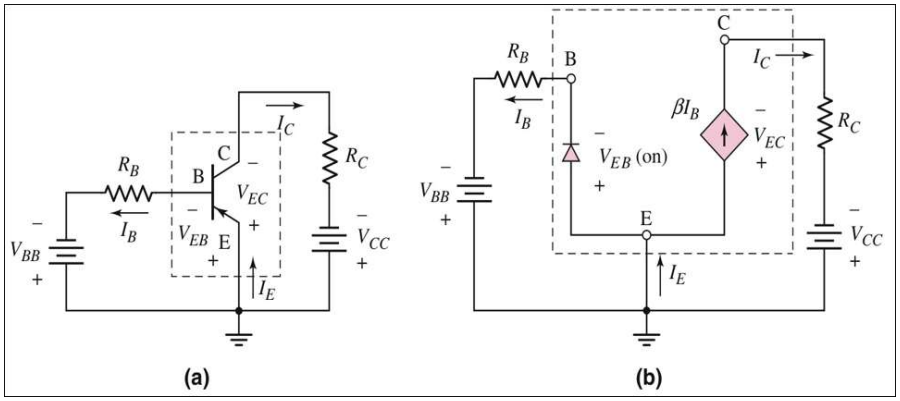
Early Voltage/Finite Output Resistance



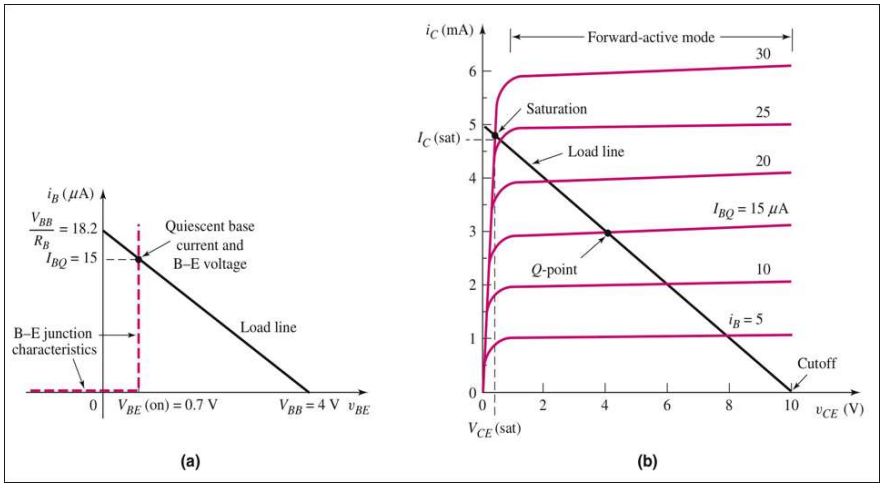
DC Equivalent Circuit for npn C-E



DC Equivalent Circuit for pnp C-E



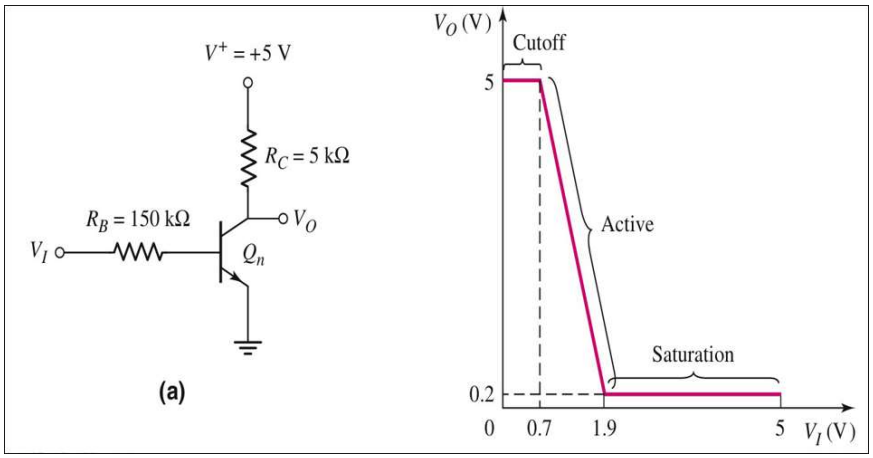
Load Line



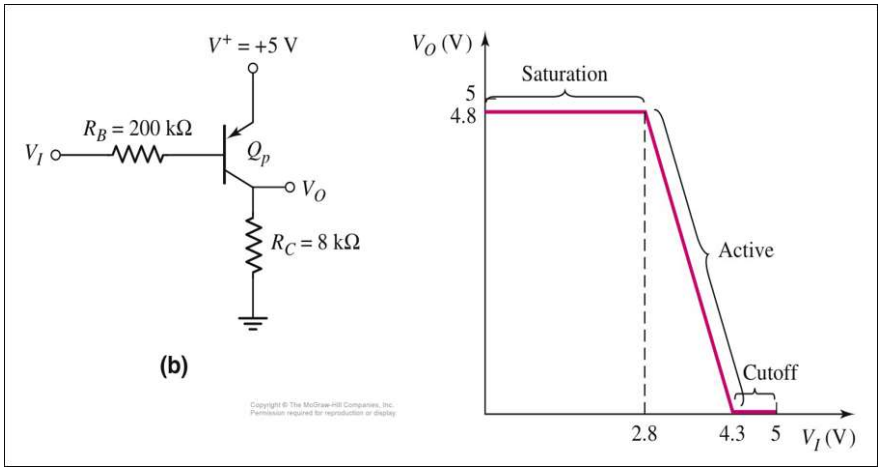
Problem-Solving Technique: Bipolar DC Analysis

1. Assume that the transistor is biased in forward active mode
   a. $V_{BE} = V_{BE}(on)$, $I_B > 0$, & $I_C = \beta I_B$
2. Analyze 'linear' circuit.
3. Evaluate the resulting state of transistor.
   a. If $V_{CE} > V_{CE}(sat)$, assumption is correct
   b. If $I_B < 0$, transistor likely in cutoff
   c. If $V_{CE} < 0$, transistor likely in saturation
4. If initial assumption is incorrect, make new assumption and return to Step 2.

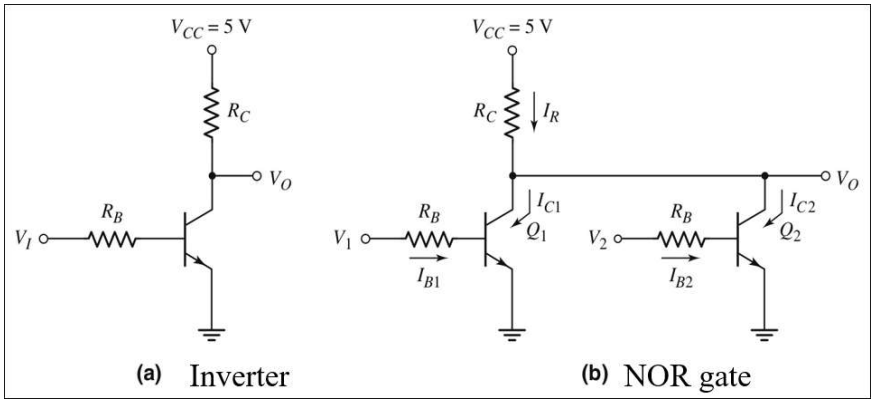
Voltage Transfer Characteristic for npn Circuit



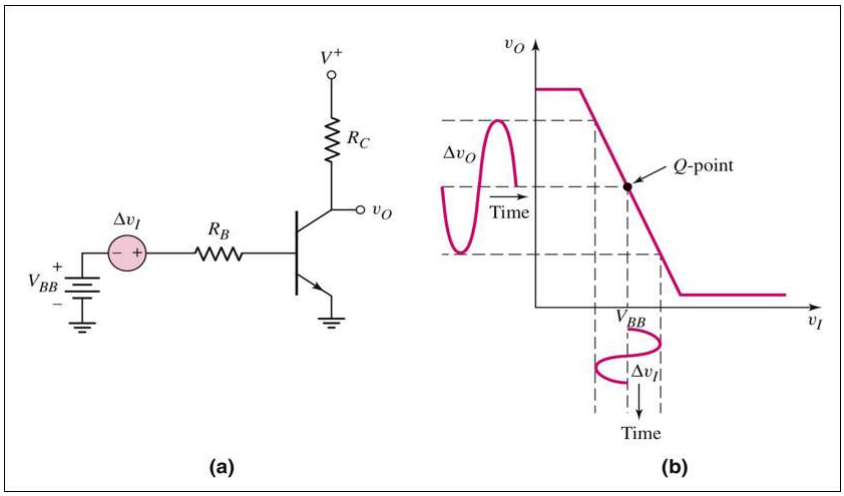
Voltage Transfer Characteristic for pnp Circuit



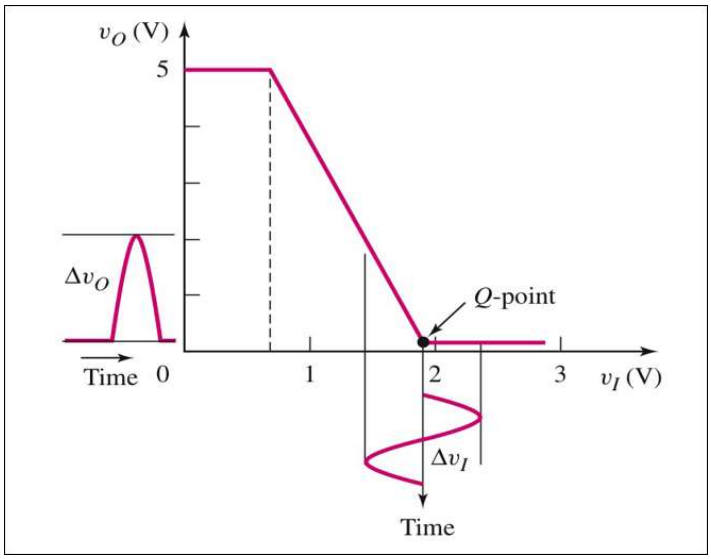
Digital Logic



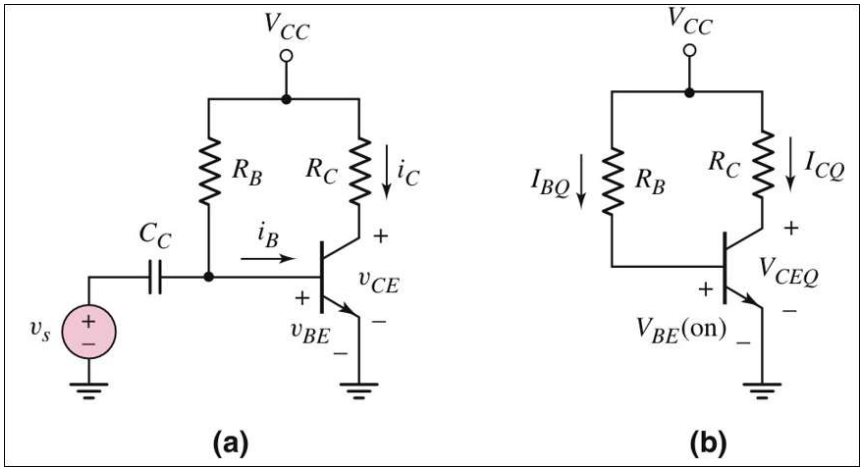
BT as Inverter



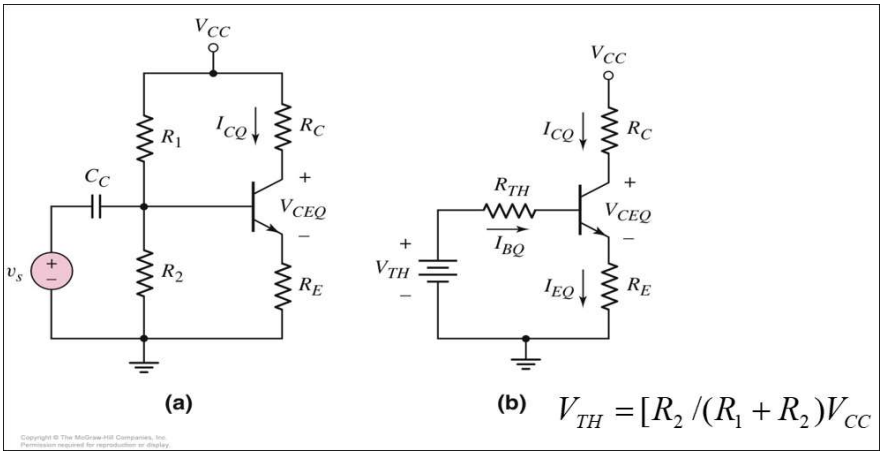
Effect of Improper Biasing on Amplified Signal Waveform



Single Base Resistor Biasing

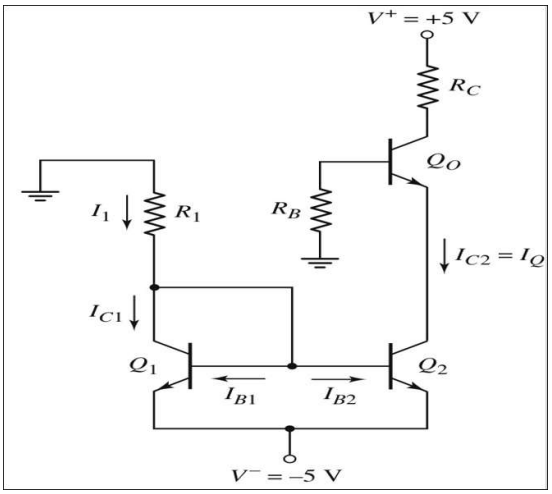


C-E with Voltage Divider Biasing and Emitter Resistor



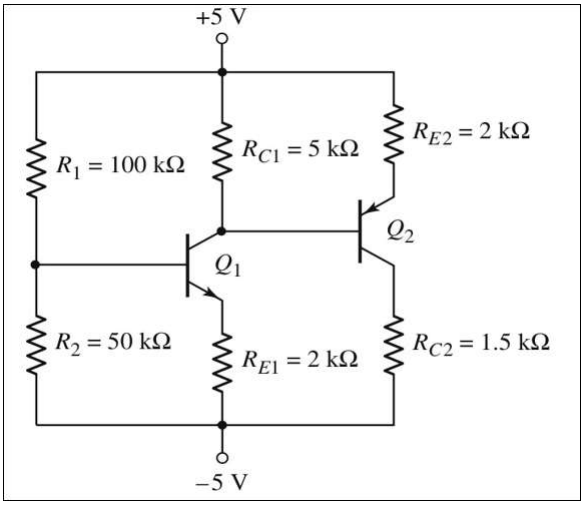
$$V_{TH} = [R_2 /(R_1 + R_2)V_{CC}$$

Integrated Circuit Biasing



$$I_C = I_Q = \frac{I_1}{1+\frac{2}{\beta}}$$

Multistage Cascade Transistor Circuit



Multistage Cascode Transistor Circuit