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VACASK – a novel analog integrated circuit simulator

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What is VACASK

- Verilog-A Circuit AnalySis Kernel
- Analog circuit simulator
- Spectre-like input syntax
- Modern C++
- Short (44k lines)
- Easy to extend
- Verilog-A device models
- OpenVAF Verilog-A compiler
  https://github.com/arpadbuermen/OpenVAF
- KLU linear solver

https://codeberg.org/arpadbuermen/VACASK

```
CMOS ring oscillator

load “psp103v4.osdi”
include “cmos_models.inc”
model isrc isource
model vsrc vsource

subckt inv(in out vdd vss)
parameters w=10u l=0.2u fac=2
  mp (out in vdd vdd) pmos w=w*fac l=l
  mn (out in vss vss) nmos w=w l=l
ends

subckt ring()
  x1 (1 2 vdd 0) inv
  x2 (2 3 vdd 0) inv
  x3 (3 1 vdd 0) inv
ends

vdd (vdd 0) vsrc dc=1.2

subckt start()
  ipulse (0 1) isrc type=”pulse” v0=0 v1=1u delay=1n rise=1n fall=1n width=1n
ends

control
  elaborate circuit(“ring”, “start”)
  analysis tran1 tran step=0.05n stop=1u maxstep=0.05n
endc
```

Features

- Model/analysis separation
- SPICE analyses + HB
- Parameterized, hierarchical
- Sweep anything
- Alter parameters wo. restart
- Change topology wo. restart
- Precise (residual checks)
- Fast (designed for modern CPUs)
- Xschem schematic editor
- IHP OpenPDK (SG13G2 node)

```
// ring oscillator definition here ...

control
  elaborate circuit(“ring”, “start”) // with startup pulse
  analysis tran1 tran step=0.05n stop=1u maxstep=0.05n

  elaborate circuit(“ring”) // no startup pulse
  analysis tran2 tran step=0.05n stop=1u maxstep=0.05n

  postprocess(PYTHON , “runme,py”)
endc

embed “runme.py” <<<FILE
  from rawfile import rawread
  import numpy as np
  import matplotlib.pyplot as plt

  fig1, ax1 = plt.subplots(2, 1)

  tran1 = rawread('tran1.raw').get()
  t = tran1["time"]; v1 = tran1["1"]
  fig1.axes[0].set_title('Oscillator startup, without a pulse')
  fig1.axes[0].plot(t*1e6, v1, color="blue", marker=".", label="v(1)")

  tran2 = rawread('tran1.raw').get()
  t = tran2["time"]; v1 = tran2["1"]
  fig1.axes[0].set_title('Oscillator startup, with a pulse')
  fig1.axes[1].plot(t*1e6, v1, color="blue", marker=".", label="v(1)")

  plt.show()
>>> FILE
```

OpenVAF Verilog-A compiler

- Free (GPL V3) Verilog-A compiler.
- Author: Pascal Kuthe
- Revived as OpenVAF-reloaded (2024)
- Can handle all public Compact Model Coalition (CMC) models, supports large part of Verilog-A.
- Represents model with a generic system of equations, not limited to SPICE.
- Optimizes equations using modern compiler techniques.
- Fast (usually below 1s), LLVM-based, generates highly optimized machine code.
- Written in Rust.

https://github.com/arpadbuermen/OpenVAF-reloaded

Compilation time in seconds for various Verilog-A models

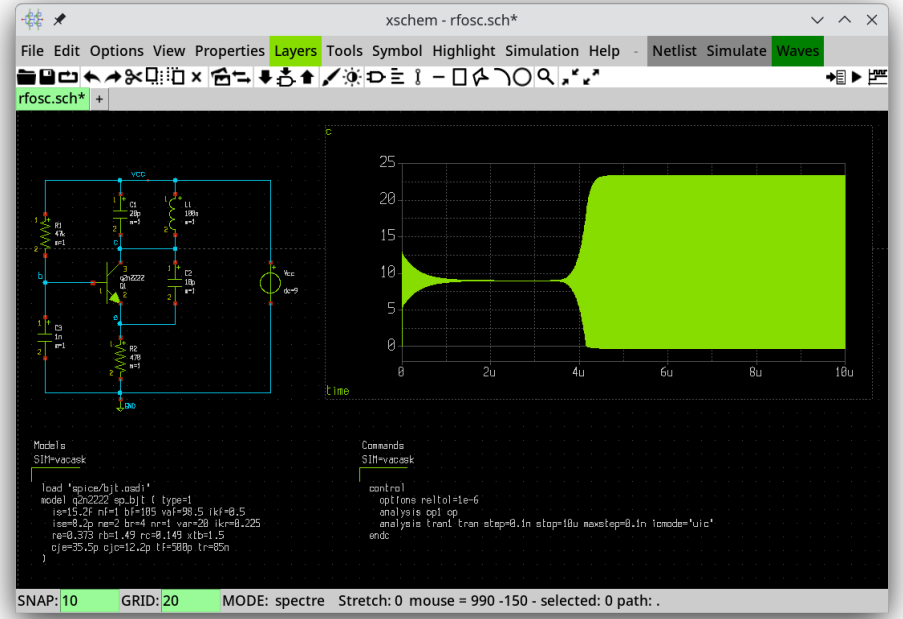
	PSPv103	BSIM4	EKV2.6	JUNCAP200	HICUM/L2v3.0
OpenVAF	3.48	6.7	0.23	0.61	0.72
Xyce ADMS	109	25.1	9.6	16.6	22
ADS	33.9	27.0	2.5	5.1	7.7
Spectre	27.4	-	6.1	11.4	19.7

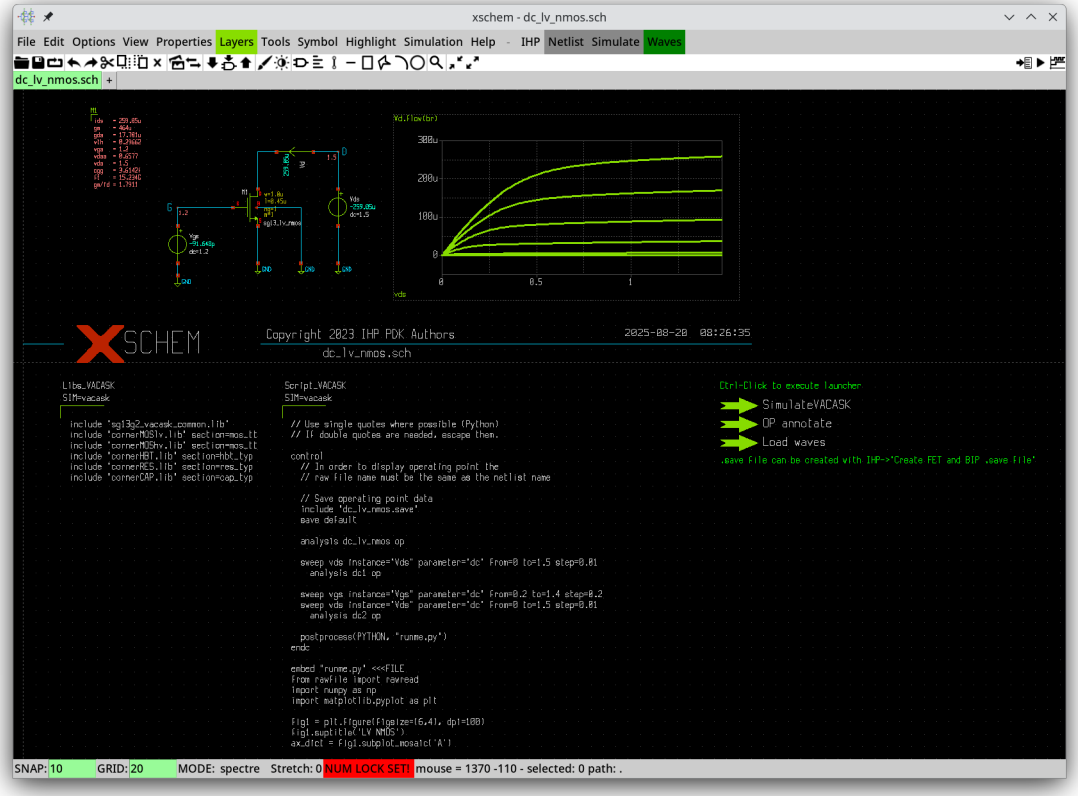
Runtime of HICUM/L2v2p4p0 characteristics simulation

Case	Time [s]	Case	Time [s]
Ngspice (OpenVAF)	9.16	**ADS (Verilog-A)**	8.63
Ngspice (builtin)	14.64	**ADS (builtin)**	7.01
Xyce (ADMS)	36.42	**Spectre (Verilog-A)**	52.61
Xyce (builtin)	26.56	**Spectre (builtin)**	25.33

Source: https://openvaf.semimod.de/docs/details/performance/

Xschem schematic editor integration





Benchmark results 1/3

RC with pulsed excitation

Simulator	Time [s]	Points	Evals
Xyce	9.39	1011527	2029571
Xyce – fast	4.12	1011527	2209571
Gnucap	8.54	1006982	2018061
Ngspice	1.31	1006013	2012031
VACASK	0.94	1005006	2010014

Graetz rectifier with RC load

Simulator	Time [s]	Points	Rejected	Evals
Xyce	10.60	1000002	0	2000014
Xyce – fast	5.34	1000002	0	2000014
Gnucap	15.16	1000026	12	3459503
Ngspice	2.21	1000008	0	2000024
VACASK	1.89	1000003	0	2000277

Voltage multiplier (diode ladder)

Simulator	Time [s]	Points	Rejected	Evals
Xyce	5.51	502341	1270	1041833
Xyce – fast	2.78	502341	1270	1041833
Gnucap	9.94	520797	739	2300992
Ngspice	1.16	500467	957	1019733
VACASK	0.97	500056	3	1001217

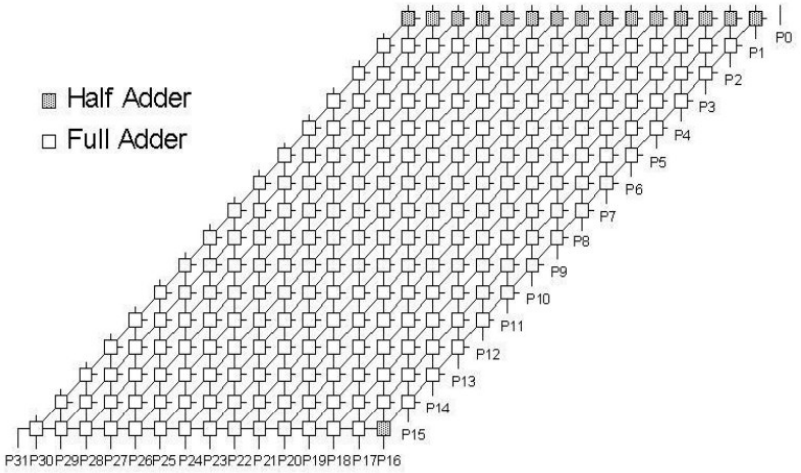
Evals … number of circuit evaluations

9-stage ring oscillator (PSP103.4)

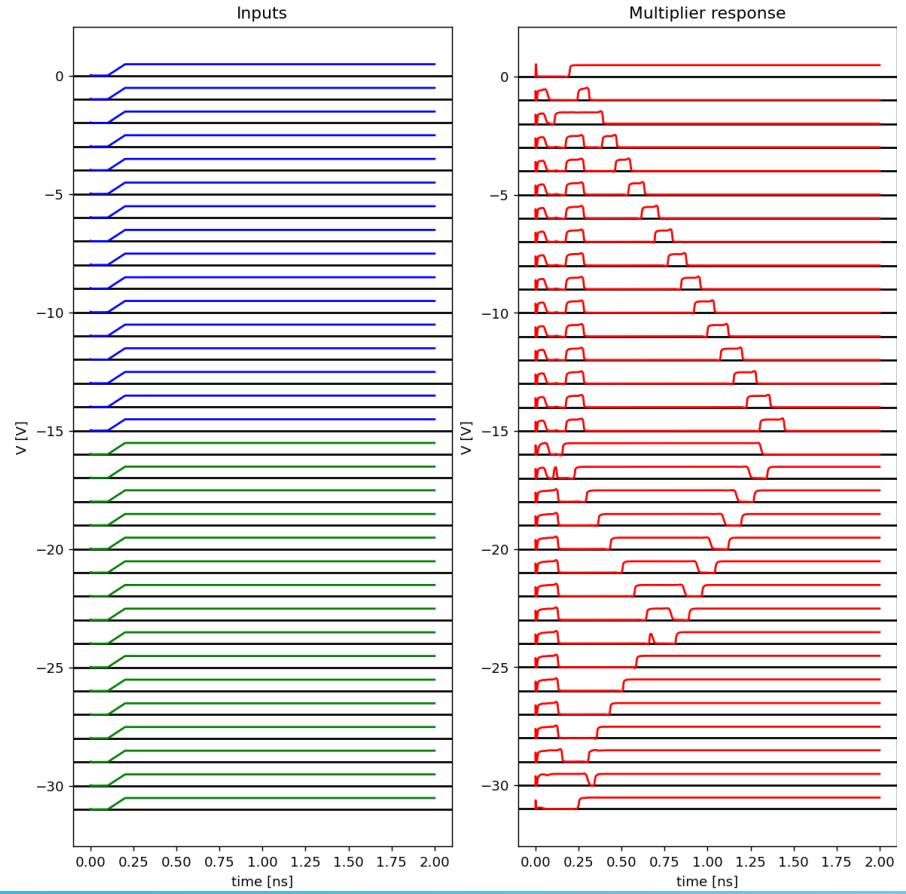
Simulator	Time [s]	Points	Rejected	Evals
Xyce	3.33	27310	0	95462
Xyce – fast	3.10	27310	0	95462
Ngspice	1.60	20556	1037	80018
VACASK	1.18	26066	0	81875

Benchmark results 2/3

C6288: 16x16 digital multiplier
Compute 0xFFFF x 0xFFFF
PSP103.4 MOSFETs
10112 transistors, 25380 unknowns



https://codeberg.org/arpadbuermen/VACASK/src/branch/main/...
...benchmark/c6288/vacask/runme.sim



Benchmark results 3/3

Default VACASK settings

Residual tolerance checks enabled
Continuation bypass enabled

Simulator	Time [s]	Points	Rejected	Evals
Xyce	151.57	1013	37	3559
Ngspice	71.81	1020	1	3474
VACASK	57.98	1021	7	3487

Modified VACASK settings

Residual tolerance checks disabled
Effect of continuation bypass (cb)

Simulator	Time [s]	Points	Rejected	Evals
Ngspice	71.81	1020	1	3474
VACASK, no cb	63.19	1024	8	3090
VACASK	48.34	1024	8	3090

Modified VACASK settings

Effect of residual tolerance checks (rtc)
No rtc == precision of SPICE

Simulator	Time [s]	Points	Rejected	Evals
Ngspice	71.81	1020	1	3474
VACASK	57.98	1021	7	3487
VACASK, no rtc	48.34	1024	8	3090

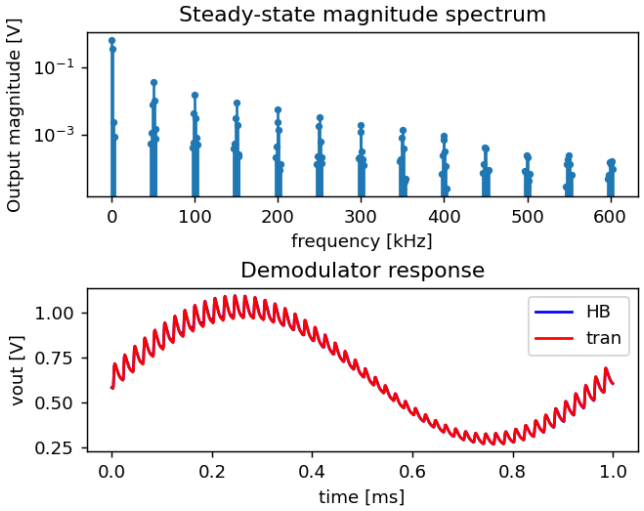
Modified VACASK settings

Residual tolerance checks disabled
Effect of inactive element bypass (ieb)

Simulator	Time [s]	Points	Rejected	Evals
Ngspice	71.81	1020	1	3474
VACASK	48.34	1024	8	3090
VACASK, ieb	46.74	1024	10	3101

Harmonic balance - examples

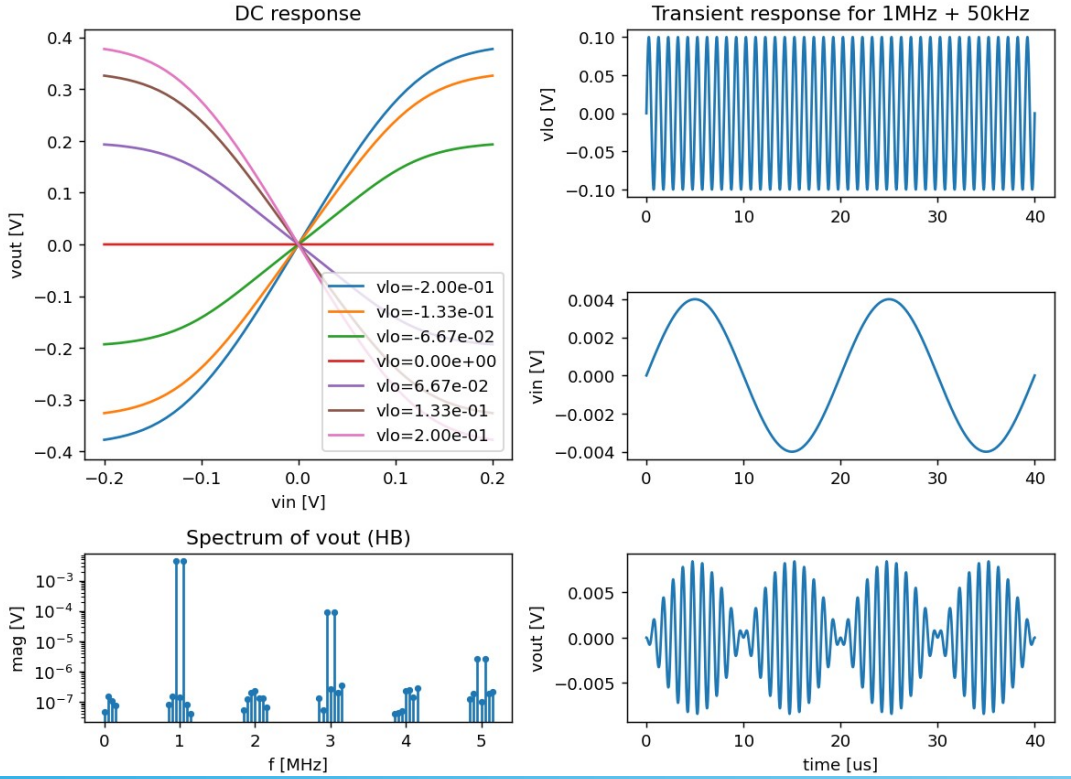
Diode AM demodulator, 2 tone HB, 3 sidebands
diode + R + C
50kHz carrier, 1.01kHz signal (incommensurate)



https://codeberg.org/arpadbuermen/VACASK/...
...src/branch/main/test/test_hb5.sim

https://codeberg.org/arpadbuermen/VACASK/...
...src/branch/main/demo/gilbert/gilbert.sim

Gilbert cell mixer, 2 tone HB, 3 sidebands
6 MOSFETS (PSP103.4), 3 resistors



Builtin, legacy (SPICE3), and modern devices

- Builtins: voltage & current source, linear controlled sources
- Modern devices: Verilog-A, supported through OpenVAF
  BSIMBULK, BSIM-CMG, BSIM-IMG, PSP, HICUM, VBIC, ...
- SPICE3 devices converted into Verilog-A:
  resistor, capacitor, inductor, diode (levels 1 and 3)
  JFET L1-2, MESFET L1, Gummel-Poon BJT,
  MOSFET L 1-3, 6, 9, BSIM3 3.3.0, BSIM4 4.8.3
- TODO: old versions of BSIM3&4, BSIMSOI
- Verilog-A Distiller
  https://codeberg.org/arpadbuermen/VADistiller

Roadmap

- Create a FOSS alternative to commercial RF simulators like Spectre and ADS.
- Convert Skywater PDK
- Faster NOISE and XF analyses (adjunct circuit equations)
- Stability analysis (STAB) and S-parameter analysis (SP)
- Transient noise analysis
- Parallel evaluation (OpenMP), parallel linear solver (MUMPS, SUPERLU?)
- Shooting (PSS) & small-signal family (PAC, PXF, PNOISE, PSP, PSTAB)
- Improve harmonic balance, use FFTW library
- Convolutional linear models (defined in frequency domain, i.e. touchstone)

Thank you.