Call for Papers

Test and Reliability Track at DATE 2016

International Congress Center Dresden, Germany, March 14–18, 2016

The **Design, Automation and Test in Europe conference and exhibition** is the main European event bringing together designers and design automation users, researchers and vendors, as well as specialists in the hardware and software design, test and manufacturing of electronic circuits and systems.

One of the tracks of DATE is devoted to **Methods, Tools and Innovations for Testing and Reliability of Electronic Circuits and Systems**. You are invited to submit your research contributions to the test and reliability track.

This five-day event consists of a **conference** with plenary keynotes, regular papers, interactive presentations, panels and hot-topic sessions, tutorials, master courses and workshops. The scientific conference is complemented by a commercial **exhibition** showing the state-of-the-art in design and test tools, methodologies, IP and design services. Both the conference and the exhibition, together with the many user group meetings, fringe meetings, university booth and social events offer a wide variety of opportunities to meet and exchange information.

TOPICS

T1 Defects, Faults, Variability and Reliability Analysis and Modeling

Chairs: Rob Aitken (ARM, US), Michel Renovell (LIRMM, FR)

Identification, characterization and modeling of defects, faults and degradation mechanisms; defect-based fault analysis; reliability analysis and modeling, failure mode and effect analysis (FMEA) and physics of failures; noise and uncertainty modeling; test and reliability issues in emerging technologies; modeling and mitigation of physical sources of errors such as process, voltage, temperature and aging variations; process yield modeling and enhancement; design-for-manufacturability and design-for-yield.

T2 Test Generation, Simulation and Diagnosis

Chairs: Bernd Becker (University of Freiburg, DE), Wu-Tung Cheng (Mentor Graphics, US)

Test pattern generation (TPG); fault simulation; system test; test coverage metrics and estimation; adaptive test; self-healing/self-calibration/self-adaptation; diagnosis; debug; post-silicon validation; testing at various levels of a system: embedded core, System-on-Chip, System-in-Package, 3D chips; hardware/software system test; processor based test.

T3 Design-for-Test, Test Compression and Access

Chairs: Paolo Prinetto (Politecnico di Torino, IT), Magdy Abadir (Freescale Semiconductor, Inc., US)

Design-for-test, built-in self-test and built-in diagnosis; synthesis for testability; test resource partitioning, embedded test; test data compression; scan-based test and diagnosis; BIST for memories and regular structures, low power DFT techniques, DFT for secure systems, DFT economics; industrial test: test equipment, including ATE hardware and software, probe stations, handlers; multi-site testing; economics of test; case studies, test economics.

T4 On-Line Test, Fault Tolerance and Robust Systems

Chairs: Fabrizio Lombardi (Northeastern University, US), Cristiana Bolchini (Politecnico di Milano, IT)

Transient fault evaluation; soft error susceptibility; on-line testing and fault tolerance for signal integrity; concurrent monitors and diagnosis; coding techniques; in-field testing and diagnosis; on-line testing; high availability systems; secure and safe circuit and system design; dependability evaluation, reliable system design; hardware/software recovery; self-repair; fault tolerance.

DT5 Design and Test for Analog and Mixed-Signal Circuits and Systems

Chairs: André Ivanov (University of British Columbia, CA), Helmut Graeb (Technische Universität München, DE)

Layout and topology generation; architecture, system and circuit synthesis and optimization; formal and symbolic techniques; hardware description languages and models of computation; innovative circuit topologies and architectures; self-healing and self-calibration; test generation; fault modeling and simulation; built-in self-test; design-for-test; fault diagnosis; defect characterization and failure analysis; on-line test and fault tolerance; design-for-manufacturability and design-for-yield; test metrics and economics.

PAPER SUBMISSION

All manuscripts must be submitted electronically before **Sunday, September 13, 2015**, following the instructions on the conference web page:

www.date-conference.com

The accepted file format is PDF. Any other format and manuscripts received in hard-copy form will not be processed.

Papers can be submitted for either formal oral presentation or for interactive presentation. Oral presentations require novel and complete research work supported by experimental results. Interactive presentations are expected to articulate emerging and future design, verification and test problems including work in progress and identify open problems that merit innovative future research. These presentations are given on a laptop in a face-to-face discussion area.

Submissions should not exceed 6 pages in length for oral-presentation papers and 4 pages in length for interactive-presentation papers, and should be formatted as close as possible to the final format: A4 or letter sheets, double column, single spaced, Times or equivalent font of minimum 10pt (templates are available on the DATE website for your convenience). To permit blind review, submissions should not include the author names. Any submission not in line with the above rules will be discarded.

All papers will be evaluated with regard to their suitability for the conference, originality, and technical soundness. The Programme Committee reserves the right to reorient oral-presentation papers to interactive-presentation and vice versa, to obtain the most suitable presentation format.

INFORMATION

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