MODELING AND SIMULATION OF MOS TRANSISTOR MISMATCH

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Abstract

The paper is an overview of MOS transistor mismatch modeling and simulation over the existent literature. The fluctuations of physical parameters and line width are the main causes of mismatch. There are two types of mismatch. Systematic mismatch can be reduced to great extent with proper layout. Different patterns are available, that are able to reduce from linear to n-th order polynomial systematic mismatch. Stochastic mismatch can only be reduced with better process control and larger transistor areas. There are different approaches for calculating the standard deviation representing stochastic mismatch. Simple formulas (e.g. square root of area rule) are most commonly used. With the reducing of the transistor area some new effects should be considerate and more complex formulas are needed. On the other hand correlation functions and frequency domain analysis with spatial spectra give more accurate results. These two approaches are more general but they do not give physical insight and the final layout should be known. Mismatch can be simulated in several ways. Brute force simulation based on Monte-Carlo analysis is appropriate for any kind of distribution but it is the most time expensive. Simulations based on small signal analysis are faster because less circuit simulations are needed to calculate the sensitivity. Two different approaches to calculate the sensitivity are presented in this paper.

Keywords: MOS transistor mismatch, simulation, modeling

Presenting Author's Biography

Gregor Cijan. Received the uni. dip. ing. degree in electrical engineering from the University of Ljubljana in 2006. Since 2006 he has been a junior researcher with the Regional Development Agency of Northern Primorska. Currently he is a Ph.D. student at the Faculty of Electrical engineering, University of Ljubljana. His research interests include circuit simulation, circuit optimization, and modeling and simulation of device mismatch.

1 Introduction

The paper is an overview of MOS transistor mismatch modeling and simulation. Mismatch is an effect that arises in IC fabrication and is a limiting factor of the accuracy and reliability of many analog and digital integrated circuits. Due to mismatch two equally designed (drawn) transistors display different electrical behavior due to mismatch. The main reason for the differences is the non-uniformity of process parameters across the wafer. Mismatch affects electrical parameters of the transistor, which in turn differ between two identically drawn devices. Consequently the operating point and other circuit characteristics differ from their desired values.

The first studies on MOS technology mismatch were done in the early 80's on capacitors [1, 2]. Later study of mismatch was extended to MOS transistor because not all high speed precision circuits can be designed with matching capacitor technique. The first researches of MOS transistors matching identified some sources of mismatch [3] and defined a model that expressed the standard deviation of threshold voltage (V_t) and current factor (β) with the physical parameter of the MOS transistor [4]. A general parameter mismatch variance model was presented by Pelgrom et al. [5] in 1989. This simple model represented the reference for mismatch modeling in analog integrated circuits for a decade.

The rest of the paper is organized as follow: In Section 2 two types of mismatch effect are presented. Further section 3 describe different way of mismatch modeling and in section 4 some common approaches to simulate mismatch are shown.

2 Stochastic and systematic mismatch

The main reason for MOS transistor mismatch is the stochastic nature of the fabrication process. After the dies are produced some additional mismatch is added during the die bonding [6]. In general mismatch can be divided in two components: a local (statistical) and a global (stochastic) component.

2.1 Stochastic

The main reason for the statistical component is the variation of the fabrication process, caused by random microscopic device architecture fluctuations, such as statistical variations in the number of dopant atoms, built-in electrical charges, gate-oxide thickness, edge roughness, etc.

Stochastic mismatch can only be reduced with better process control and larger transistor areas. The W/L ratio also influences transistor mismatch. In [7] it was shown how matching can be improved without changing the layout area. Better matching is obtained if the ratio. This, however, reduce the switching speed. Because of this weakness the approach is not frequently used.

2.2 Systematic

Some possible reasons for the systematic component are non-uniform thermal distribution during the fabrication process, lens aberration during the photolithographic process, etc. The systematic component is deterministic and also a model is available in [8], but because the placement and the orientation of the transistor on the die and within the wafer are unknown in the design phase, it is also often modeled as a stochastic process.

Systematic mismatch can be reduced to great extent with proper layout. For the best matching of two equally designed devices they should be as close as possible with their wider side in parallel. In Fig. 1. The transistors pair 1 and 3 matches better than 1 and 2. Much better results can be achieved by dividing a transistor in smaller devices connected in parallel that are arranged in different patterns [9]. Three different layout techniques capable of canceling systematic mismatch error due to higher-order gradient effects are presented in [10]. These are central symmetry pattern (Fig. 2 a-f), circular symmetry pattern (Fig. 2 g) and hexagonal tessellation (Fig. 2 h). The n-th order central symmetry and n-th order circular symmetry can cancel mismatch from linear to the n-th order polynomal between two devices by using 2^n unit cells for each one. The hexagonal tessellation has a higher area-efficiency because it can cancel quadratic gradient with only 3 units per device.

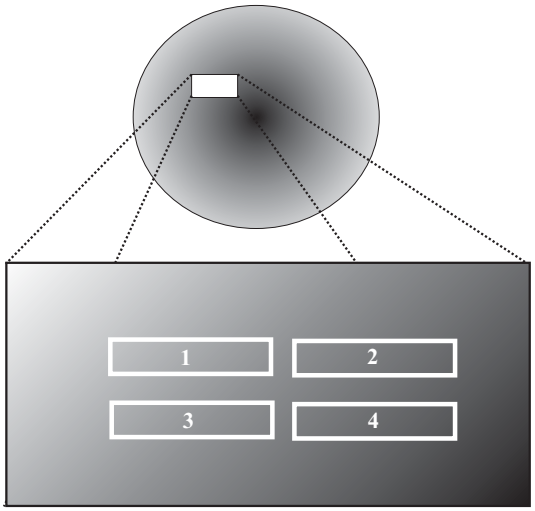

Fig. 1 Systematic mismatch area

3 Modeling

Random variations of physical parameters result in randomly distributed MOS transistor model parameters. Most often the Gaussian distribution is used for modeling the stochastic variations of model parameters. The amount of mismatch can be expressed with standard deviations (σ) of transistor model parameters. There are different approaches for calculating this standard deviation. Simple formulas (e.g. square root of area rule) are

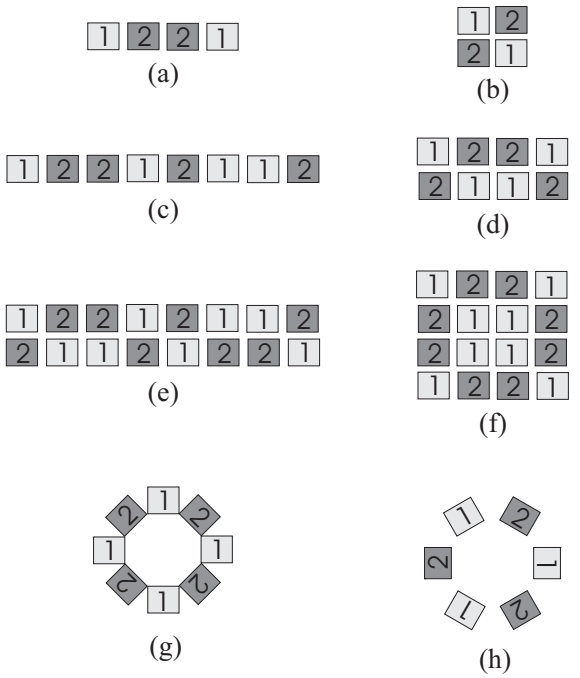

Fig. 2 Pattern to reduce systematic mismatch. 1 and 2 denote the smaller devices that constitute transistors 1 and 2.

most commonly used. On the other hand correlation functions, and frequency domain analysis with spatial spectra give more general results.

3.1 Simple Formulas

In 1986 Lakshmikumar et all. [4] described the MOS transistor mismatch model for the standard deviation of the threshold voltage (V_T) and current factor (β), which was derivered from the physical sources of mismatch. In 1989 Pelgrom [5] proposed a more general model based on mathematical treatment done in the frequency domain, and not in the spatial domain as Lakshmikumar did. The model takes into account local process variations (characterized by spatial white noise) and global proces variation (characterized by a single spatial frequency inversely proportional to the wafer diameter). The standard deviation of a parameter difference (ΔP) between two identically drawn transistors is expressed by Eq. (1),

$$\sigma^2(\Delta P) = \frac{A_p^2}{WL} + S_p^2 \cdot D^2 \qquad (1)$$

where A_P and S_P are technology-dependent parameters, W and L are channel dimensions, and D is the distance between two transistors. Most commonly used transistor parameters in mismatch modeling are threshold voltage (V_T) and current factor (β), although some models use additional parameters [11].

3.2 Short and narrow channels

The model presented in (1) is a good approximation for transistor sizes above $2\mu m$. For short and narrow channel transistors built in $0.7\mu m$ CMOS technology some new effects must be considered and additional terms appear in Eq. (2) and Eq. (3) [5, 12]. For small geometry MOS devices the channel depletion tickness can no loger be considered uniform. The depletion charge variance contributes a $\frac{1}{WL^2}$ term and a $\frac{1}{W^2L}$ term resulting in a new mismatch model for threshold voltage (2).

$$\sigma^2(\Delta V_t) = \frac{A_{1V_t}^2}{WL} + \frac{A_{2V_t}^2}{WL^2} - \frac{A_{3V_t}^2}{W^2L} + S_{V_t}^2 D^2 \qquad (2)$$

An extendent current factor mismatch model (3) has been presented in [5]. Pelgrom predicted that for short and narrow channel devices the edge roughness effect becomes important and appears as additional terms in the current-factor variance.

$$\sigma^2\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_{1\beta}^2}{WL} + \frac{A_{2\beta}^2}{WL^2} + \frac{A_{3\beta}^2}{W^2L} + S_\beta^2 D^2 \qquad (3)$$

For big devices the two terms $\left(\frac{1}{W^2L}\right.$ and $\left.\frac{1}{WL^2}\right)$ in Eq. (2) and (3) can be neglected and model (1) is obtained [5]. The last term in Eq. (2) and (3) is due to gradient mismatch. The value of mismatch model (2, 3) parameters (e.g. A_{1Vt}, $A_{1\beta}$, etc.) can be obtained by processing statistical data acquired from the measurements of many dies with several transistors (different W/L values) distributed across a die.

On the other hand some physical models are also available in the literature for short channel devices. Two different approaches for modeling the short channel effect and a model that takes into account the quantum effect are presented in [13].

3.3 Frequency domain analysis with spatial spectra

A more general approach is frequency domain modeling with spatial spectra [14]. The value of a transistor parameter is obtained by integrating a noise function $p(x, y)$ representing parameters variation over the device area. The difference between a parameter of two transistors with geometries $W \times L$ at distance D is expressed with Eq. (4). For convenience it has been assumed that spacing D is along only one axes (in this case x-axis).

$$\begin{aligned}\Delta P = \frac{1}{WL}\left(\int_{-\frac{L}{2}}^{\frac{L}{2}}\int_{-W-\frac{D}{2}}^{-\frac{D}{2}} p(x,y)dydx \right. \\ \left. - \int_{-\frac{L}{2}}^{\frac{L}{2}}\int_{\frac{D}{2}}^{W+\frac{D}{2}} p(x,y)dydx\right) = \\ \frac{1}{WL}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} g(x,y)p(x,y)dxdy\end{aligned} \qquad (4)$$

If the transistor area is represented by a pulse function $g(x, y)$ (Fig. 3), the integral of $p(x, y)$ is related to the convolution between $p(x, y)$ and $g(x, y)$. By means of a two-dimensional Fourier transformation the geometry-dependent part $G(\omega_x, \omega_y)$ is separated from the mismatch generating process $P(\omega_x, \omega_y)$. With the use of Parseval's theorem the standard deviation of a parameter difference between two transistors can be expressed

with the following equation.

$$\sigma^2(\Delta P) = \int_{\omega_y=-\infty}^{\omega_y=\infty} \int_{\omega_x-\infty}^{\omega_x=\infty} |P(\omega_x,\omega_y)|^2 \cdot |G(\omega_x,\omega_y)|^2 d\omega_y d\omega_x \quad (5)$$

The Fourier transform $G(\omega_x, \omega_y)$ of $g(x, y)$ is shown in

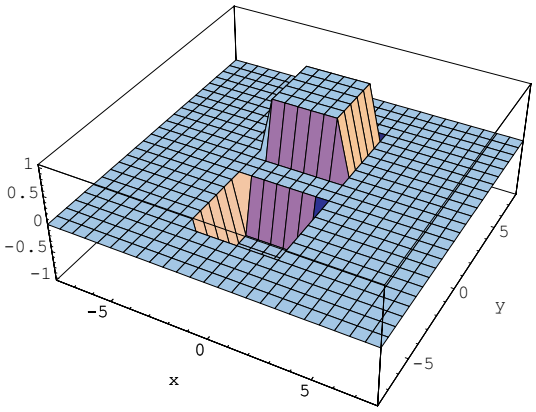

Fig. 3 $g(x, y)$-pulse function

Fig. 4b. The spectrum of the noise function $P(\omega_x, \omega_y)$

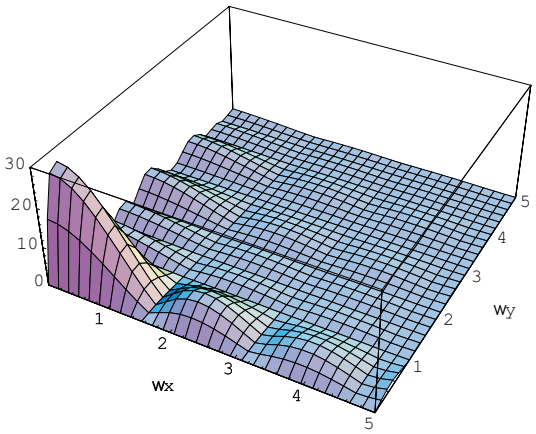

Fig. 4 $G(\omega_x, \omega_y)$-Fourier transform of the pulse function g(x,y)

are modeled with different functions and consequently different results can be obtained. A good choice is a function given by Eq. (6).

$$P_{wcn}(\omega_x,\omega_y) = \sqrt{A_P^2 + \frac{k_P^2}{\left(\omega_x^2+\omega_y^2\right)^{a_P}}} \quad (6)$$

The spectrum of the noise function P_{wcn} is composed of white noise (stochastic mismatch) and colored noise (systematic mismatch). The parameter A_P represents the white noise while parameters k_P and a_P represent the colored noise. The spectrum of the function P_{wcn} is shown in Fig. 5. Assuming only white noise ($k_P = 0$) the stadard deviation reduces to the first term of Pelgrom's model (1).

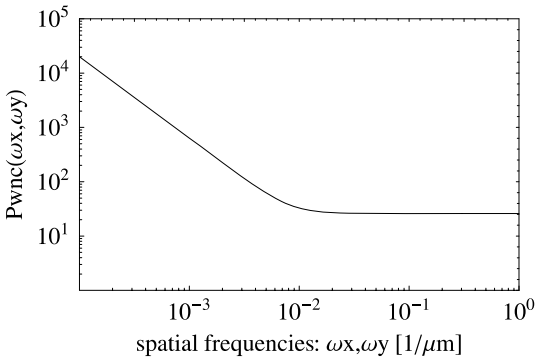

Fig. 5 Spectrum of the function (6)

The advantage of frequency domain analysis with spatial spectra is its generality. It is valid for transistors, capacitors etc. The downside of this mathematical treatment is that it does not give physical insight and that it requires the knowledge of the final layout.

3.4 Analysis by mean of correlation functions

A similar approach to frequency domain analysis with spatial spectra is the use of correlation functions [15]. The main advantages of this method is that instead of parameter standard deviation one obtains the covariance matrix $[C_{pp}]_{ij}$, that describes the joint probability distribution of parameter p across all transistors. The elements of the matrix are obtained by integrating a covariance function over the $i-th$ and $j-th$ transistors area (see Eq. (7)).

$$[\mathbf{C}_{pp}]_{ij} = \frac{1}{W_i L_i W_j L_j} \int_{x_i}^{x_i+L_i} \int_{x_j}^{x_j+L_j} \int_{y_i}^{y_i+W_i} \int_{y_j}^{y_j+W_j} C_{pp}(x_A, y_A, x_B, y_B) dx_A dx_B dy_A dy_B \quad (7)$$

The covariance function between parameter p at point $T_A(x_A, y_A)$ and point $T_B(x_B, y_B)$ is calculated using the following equation,

$$C_{pp}(x_A, y_A, x_B, y_B) = R_{pp}(x_A, y_A, x_B, y_B) - E(p(x_A, y_A)) \cdot E(p(x_B, y_B)) \quad (8)$$

where,

$$R_{pp}(x_A, y_A, x_B, y_B) = E(p(x_A, y_A)p(x_B, y_B)) \quad (9)$$

is the autocorrelation function for parameter p and $E(p(x, y))$ is the expected value of parameter p at location (x, y). For such approach the characteristics of the stochastic process $p(x, y)$ should be known. The equations (7) and (8) can be simplified if the process $p(x, y)$ is invariant under coordinate translation [15]. Consequently the expected value $E(p(x, y))$ becomes constant and the autocorrelation function depends only on the distances $\tau_{x_{ij}}$ and $\tau_{y_{ij}}$ between two points.

The results of this method depends on the choice of the autocorrelation function. Three examples are shown in

[15]. By choosing an impulse autocorrelation function (white noise)

$$R_{pp}(\tau_x, \tau_y) = b^2 \delta(\tau_x)\delta(\tau_y) \tag{10}$$

the first term of Pelgrom's model (1) is obtained. The function is composed of two Dirac functions $\delta(\tau)$ and of parameter b, which characterizes the process.

For the complete Pelgrom's model white noise with random gradient must be chosen. The autocorrelation function is calculated from (11), where parameters χ and γ are two random values.

$$p(x, y) = \chi x + \gamma \tag{11}$$

In this case the function is not translation invariant.

The best choice is a Gaussian autocorrelation function, which removes a major shortcoming of Pelgrom's model that causes the mismatch to increase beyond any limit with increasing distance. The autocorrelation function is given by

$$R_{pp}(\tau_x, \tau_y) = a_p \cdot exp[-K_{pp}^2(\tau_x^2 + \tau_y^2)] \tag{12}$$

There are many advantages of this approach: it is not limited to a pair of devices, it can be applied to any stochastic model of the process $p(x, y)$. Using this approach the cross-covariance between two different parameters of two diferent transistors can also be obtained in a similar way [15]. The lowrside are the same as those mentioned in the previous section(frequency domain analysis).

4 Simulation

Mismatch can be simulated in several different ways. The goal of mismatch simulation is to obtain the standard deviation of circuit properties caused by the stochastic nature of transistor model parameters.

4.1 Monte-Carlo simulation

Brute force simulation based on Monte-Carlo analysis is simple, precise and widely used [16, 17, 18]. Several thousand circuits with randomly chosen parameters according to the probability density function of parameter p ($pdf(p)$) are generated and simulated. The most frequently used distribution is Gaussian but the method is appropriate for any kind of distribution $pdf(p)$. It can also accomodate correlated parameters in a fairly straight forward fashion.

Before the simulation the function $pdf(p)$ for all parameters p (for example V_T and β) of all transistors in the circuit must be given. Equation (1) is a good and widely used approximation for the standard deviation of the $pdf(p)$. The mean values of electrical parameters should also be available before the simulation. If we are interested in the distribution of V_X (see Fig. 6) then the values of V_T and β for both transistor should be randomly chosen according to individual $pdf(p)$. This should be done for several thousand simulations (e.g. 10000). The results are then statistically processed in order to obtain the distributions and the standard deviation of V_X.

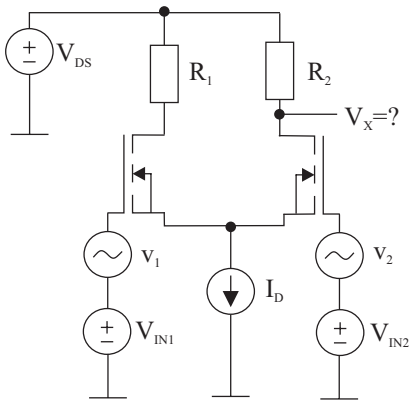

Fig. 6 A Differential pair

The downside of this method is the huge amount of computation required for the simulation of thousands of circuits.

4.2 Simulation based on small signal analysis

A faster approach than Monte-Carlo is small signal analysis. This analysis assumes that the changes caused by the stochastic nature of model parameters are within the bounds where the circuit behaves linearly. The stochastic nature of model parameters results in the variation of the MOS current which is represented by the current sources δI_{DS} connected in parallel with MOS transistor channels (Fig. 7). Normal distribution is assumed for δI_{DS}. The standard deviation of δI_{DS}

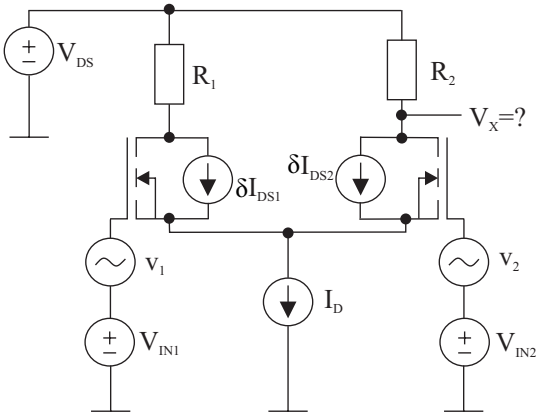

Fig. 7 A differential pair affected by mismatch.

in saturation is calculated using (13), where parameters I_{DS} and V_{GS} represent the operating point while V_T and β represent the transistor parameters.

$$\left(\frac{\sigma(\delta I_{DS})}{I_{DS}}\right)^2 = \left(\frac{\sigma(\beta)}{\beta}\right)^2 + \left(\frac{4\sigma(V_T)}{V_{GS} - V_T}\right)^2 \tag{13}$$

Eq. (13) represents a simple model [5, 19] not taking into account correlation between V_T and β. If the stan-

dard deviation od δI_{DS} are not correlated then the standard deviation of V_X can be expressed as

$$\sigma^2(V_X) = \sum_{i=1}^{n} \left(\frac{\partial V_X}{\partial \delta I_{DSi}} \right)^2 \cdot \sigma^2(\delta I_{DSi}) \qquad (14)$$

The sensitivity ($\alpha_i = \partial V_X / \partial \delta I_{DSi}$) provides the information how much the variation of I_{DSi} influences the variation of V_X. There are different ways to calculate the sensitivities of an n-transistor circuit. The heuristic approach and sensitivity analysis will be presented. A similar approach was used in [20] where the influence of process parameters on electrical parameters is calculated. Process parameters are those physically independent parameters that control the electrical behavior of a device. Electrical parameters are those that are of interest to the designer.

4.2.1 Finite difference approach

This heuristic approach takes n+1 simulations to calculate the sensitivities. One simulation is needed for the common point and n-simulations are needed for perturbed circuits. In the following equation an example for the calculation of a single sensitivity is shown.

$$\alpha_i = \frac{V_X(\delta I_{DSi}) - V_X(0)}{\delta I_{DSi}} \qquad (15)$$

4.2.2 Sensitivity analysis

A faster approach is the use of sensitivity analysis, because the circuit is solved only once for the whole set of sensitivities. This approach resembles the small signal noise analysis, where noise sources are replaced by mismatch sources. When the linearization is done and the sensitivities are known, the standard deviation of V_X is calculated using equation (14). This approach was used in [15] where not only the means for simulating the effect of mismatch on the operating piont, but also small signal AC and transiant effects of mismatch can be simulated very efficiently.

5 Example

In this example the optimization of MOS transistor mismatch is shown. The mismatch causes an opamp to exhibit offset voltage. This voltage varies randomly between different instances of the circuit. The goal was to include the offset voltage as yet another criterion in the process of circuit optimization.

Due to the limitations of the simulator (SPICE lacks support for sensitivity analysis) and the limited availability of mismatch parameters the finite difference approach with the simplest mismatch model was used. The standard deviation of the threshold voltage (V_t) and current factor (β) was calculated with the help of (16) and (17).

$$\sigma(V_t) = \frac{A_{V_t}}{\sqrt{WL}} \qquad (16)$$

$$\sigma(\beta) = \frac{A_\beta}{\sqrt{WL}} \qquad (17)$$

These two equations are based on the first term of the Pelgrom model (1). Systematic mismatch was neglected due to the assumption that the devices are located close to one another. The constants A_{V_t} and A_β for the $0.18\mu m$ technology were obtained from [21]. The offset voltage was obtained as the standard deviation of the output voltage at zero input voltage. The circuit (opamp) is depicted in Fig. 8. The results of the optimization are listed in Tab. 1. The second column contains the transistor areas and the offset voltage obtained by including mismatch effects in the set of optimization goals. The third column lists the same circuit propertis when mismatch effects were not included. It can clearly be seen that including the mismatch effects in the cost function results in the enlargement of the transistor areas and the reduction of the offset voltage. In Tab. 2 the finite difference approach is compared to the Monte-Carlo analysis with 2000 samples. The result of the finite difference approach agrees well with the result of the Monte-Carlo analysis.

Tab. 1 Comparsion of obtained transistor sizes and output offset voltage.

Transistor	With mismatch	Without mismatch
$Mn1b, Mn1, Mn4$	$11.5\mu m^2$	$8.1\mu m^2$
$Mp3$	$0.31\mu m^2$	$0.31\mu m^2$
$Mp1, Mp2$	$16.5\mu m^2$	$9.3\mu m^2$
$Mn2, Mn3$	$32.3\mu m^2$	$19.8\mu m^2$
Offset	**0.11 mV**	**0.14 mV**

Tab. 2 Standard deviation of output voltage

Approach	Obtained standard deviation
Finite difference	$0.1162mV$
Monte-Carlo	$0.1159mV$

6 Conclusion

An overview of modeling and simulation of MOS transistor mismatch has been presented. Many different models of mismatch can be found in the literature. The effect of device mismatch can be estimated using several different approaches. Only some of these approaches can be used for general purpose due to the limited availability of mismatch model parameters and limited capabilities of circuit simuators. In the given example it was shown how mismatch can be simulated and reduced by using a simple finite difference approach in conjunction with circuit optimization. The results agree well with the results of the Monte-Carlo analysis.

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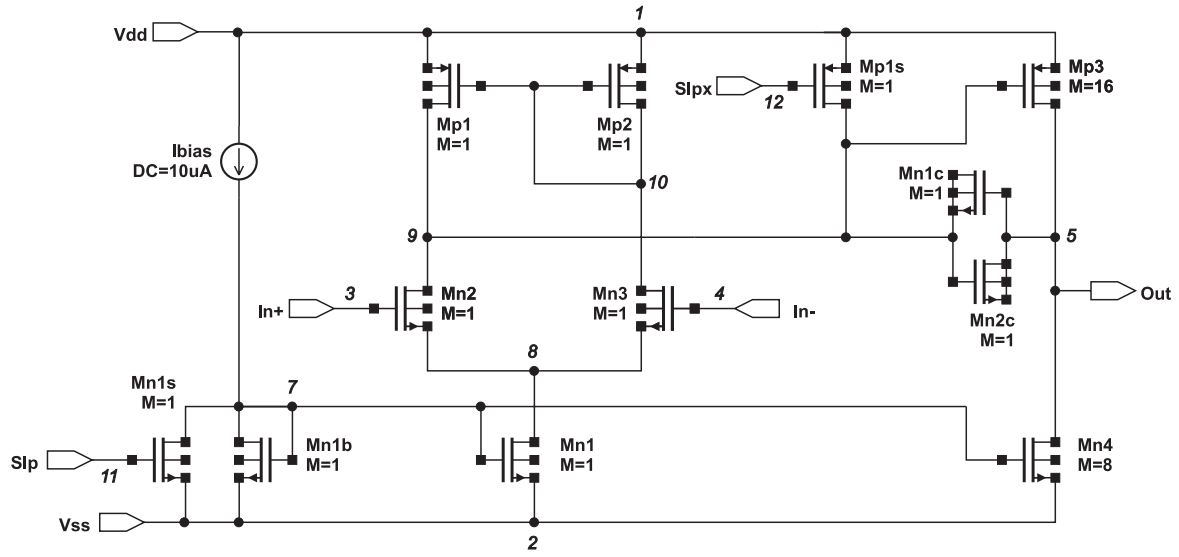

Fig. 8 A simple operational amplifer.

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